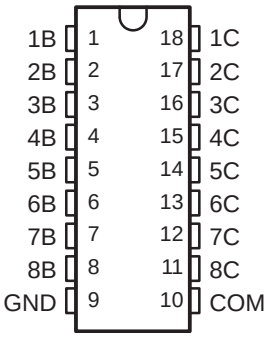
SLRS049C − FEBRUARY1997 − REVISED AUGUST 2004

- **500-mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Compatible with ULN2800A Series**

**DW OR N PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ULN2803A is a high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be connected in parallel for higher current capability.

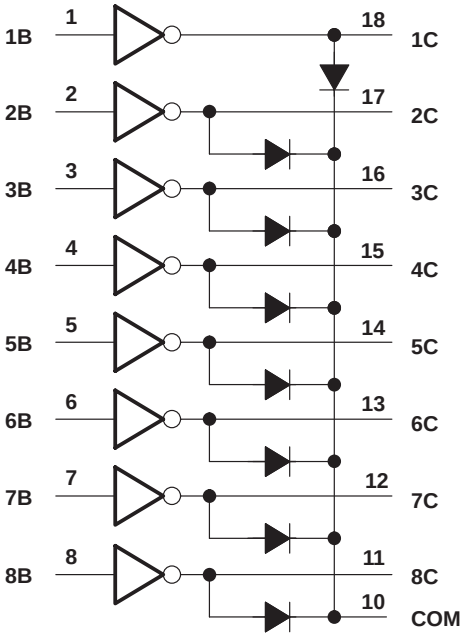
Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

**ORDERING INFORMATION**

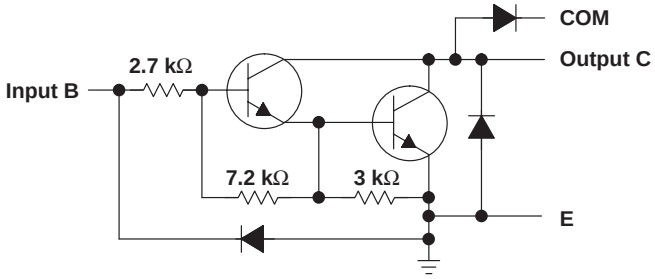
| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| −40°C to 85°C | PDIP (N) | Tube of 20 | ULN2803AN | ULN2803AN |
| | SOIC (DW) | Tube of 40 | ULN2803ADW | ULN2803A |
| | | Reel of 2000 | ULN2003ADWR | |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

## logic diagram




## schematic (each Darlington pair)



## absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage . . . . . 50 V
Input voltage (see Note 1) . . . . . 30 V
Continuous collector current . . . . . 500 mA
Output clamp diode current . . . . . 500 mA
Total substrate-terminal current . . . . . −2.5 A
Package thermal impedance, $\theta_{JA}$ (see Notes 2 and 3): DW package . . . . . TBD°C/W
N package . . . . . TBD°C/W
Operating virtual junction temperature, $T_J$ . . . . . 150°C
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.
2. Maximum power dissipation is a function of $T_J(max)$, $\theta_{JA}$, and $T_A$. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum $T_J$ of 150°C can affect reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

## electrical characteristics at 25°C free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $I_{CEX}$ | Collector cutoff current | $V_{CE}$ = 50 V, See Figure 1 | $I_I$ = 0, | | | 50 | µA |
| $I_{I(off)}$ | Off-state input current | $V_{CE}$ = 50 V, $T_A$ = 70°C, | $I_C$ = 500 µA, See Figure 2 | 50 | 65 | | µA |
| $I_{I(on)}$ | Input current | $V_I$ = 3.85 V, | See Figure 3 | | 0.93 | 1.35 | mA |
| $V_{I(on)}$ | On-state input voltage | $V_{CE}$ = 2 V, See Figure 4 | $I_C$ = 200 mA | | | 2.4 | V |
| | | | $I_C$ = 250 mA | | | 2.7 | |
| | | | $I_C$ = 300 mA | | | 3 | |
| $V_{CE(sat)}$ | Collector-emitter saturation voltage | $I_I$ = 250 µA, See Figure 5 | $I_C$ = 100 mA, | | 0.9 | 1.1 | V |
| | | $I_I$ = 350 µA, See Figure 5 | $I_C$ = 200 mA, | | 1 | 1.3 | |
| | | $I_I$ = 500 µA, See Figure 5 | $I_C$ = 350 mA, | | 1.3 | 1.6 | |
| $I_R$ | Clamp diode reverse current | $V_R$ = 50 V, | See Figure 6 | | | 50 | µA |
| $V_F$ | Clamp diode forward voltage | $I_F$ = 350 mA, | See Figure 7 | | 1.7 | 2 | V |
| $C_i$ | Input capacitance | $V_I$ = 0 V, | f = 1 MHz | | 15 | 25 | pF |

## switching characteristics at 25°C free-air temperature

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low- to high-level output | $V_S$ = 50 V, $C_L$ = 15 pF, | $R_L$ = 163 Ω, See Figure 8 | | 130 | | ns |
| $t_{PHL}$ | Propagation delay time, high- to low-level output | | | | 20 | | |
| $V_{OH}$ | High-level output voltage after switching | $V_S$ = 50 V, See Figure 9 | $I_O \approx$ 300 mA, | $V_S$ − 20 | | | mV |

## PARAMETER MEASUREMENT INFORMATION

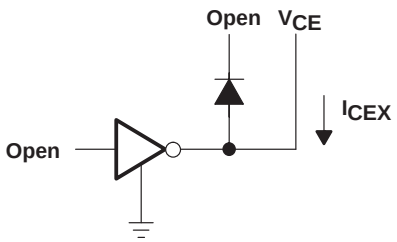



Figure 1. $I_{CEX}$ Test Circuit

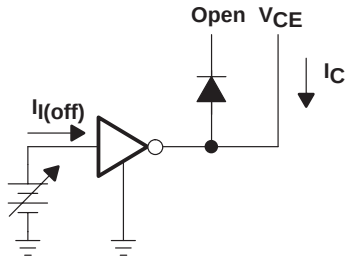



Figure 2. $I_{I(off)}$ Test Circuit

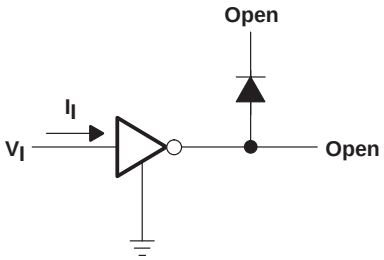



Figure 3. $I_{I(on)}$ Test Circuit

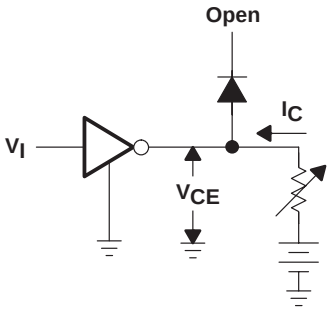



Figure 4. $V_{I(on)}$ Test Circuit

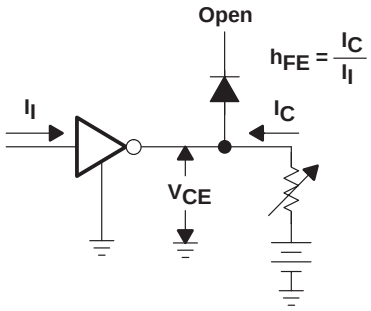



Figure 5. $h_{FE}$, $V_{CE(sat)}$ Test Circuit

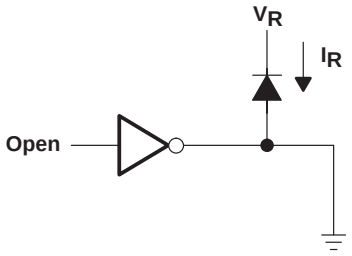



Figure 6. $I_R$ Test Circuit

## PARAMETER MEASUREMENT INFORMATION

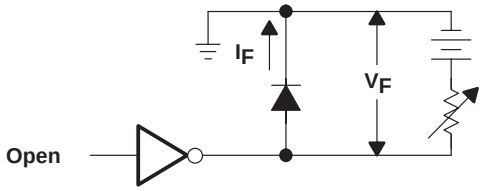
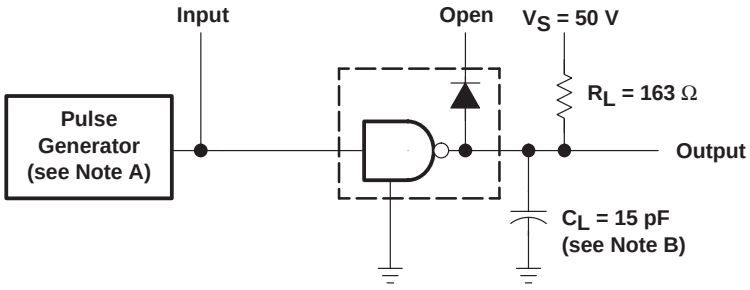
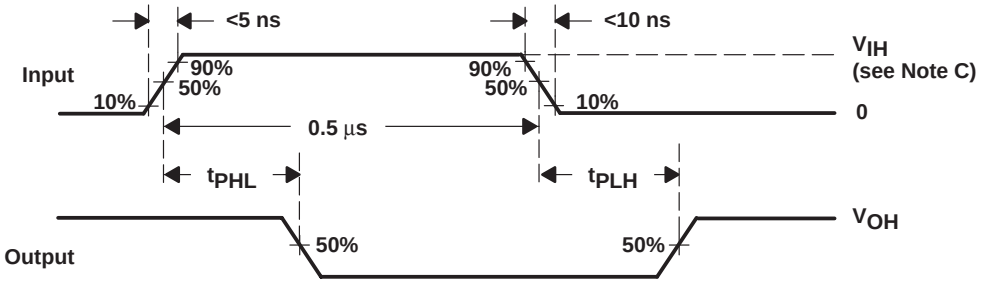



**Figure 7. $V_F$ Test Circuit**




**Test Circuit**

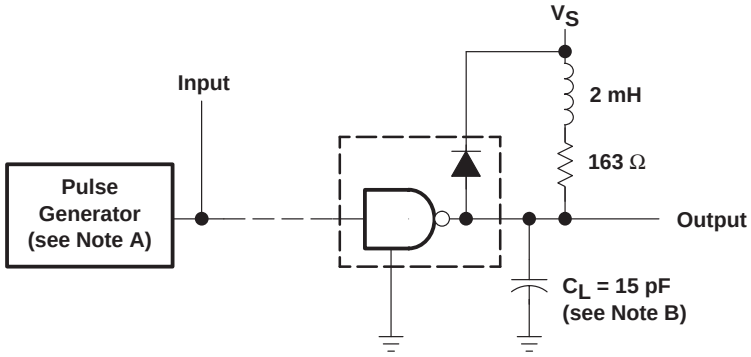



**Voltage Waveforms**

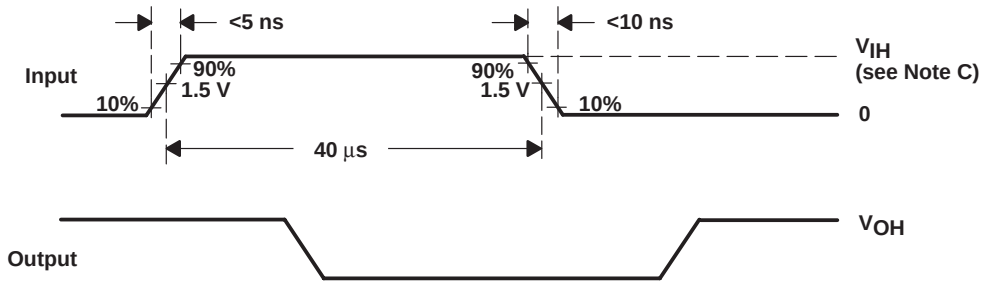
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. $V_{IH}$ = 3 V

**Figure 8. Propagation Delay Times**

## PARAMETER MEASUREMENT INFORMATION




Test Circuit

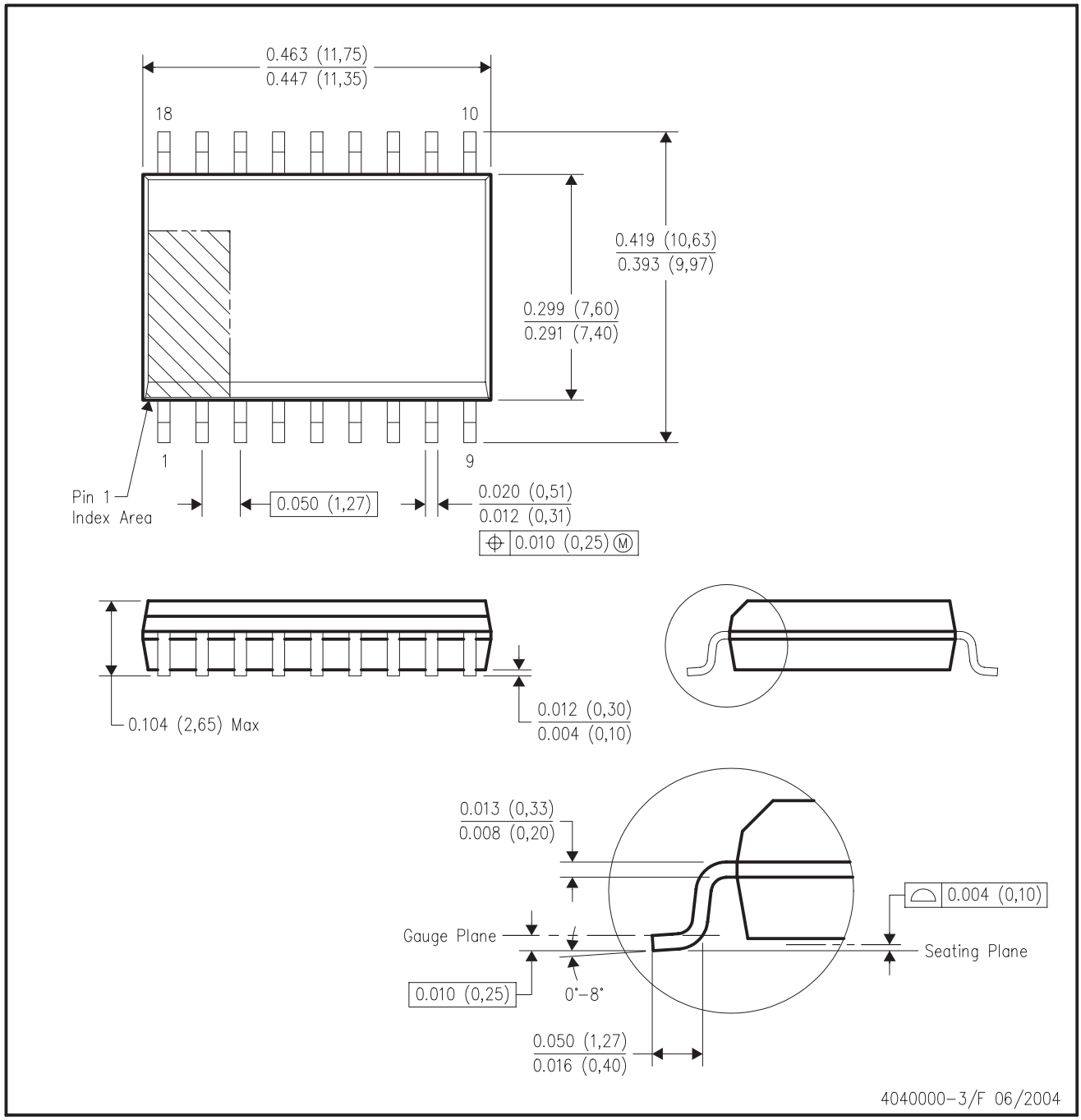



Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 KHz, $Z_O$ = 50 Ω.
B. $C_L$ includes probe and jig capacitance.
C. $V_{IH}$ = 3 V

**Figure 9. Latch-Up Test**

## DW (R–PDSO–G18) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AB.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| ULN2803ADW | ACTIVE | SOIC | DW | 18 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| ULN2803ADWR | ACTIVE | SOIC | DW | 18 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1YEAR |
| ULN2803AN | ACTIVE | PDIP | N | 18 | 20 | Pb-Free (RoHS) | CU NIPDAU | Level-NC-NC-NC |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

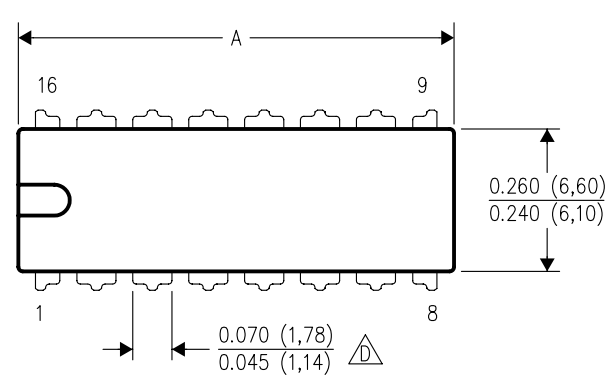
(2) Eco Plan - May not be currently available - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**None:** Not yet available Lead (Pb-Free).
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDECindustry standard classifications, and peak solder temperature.

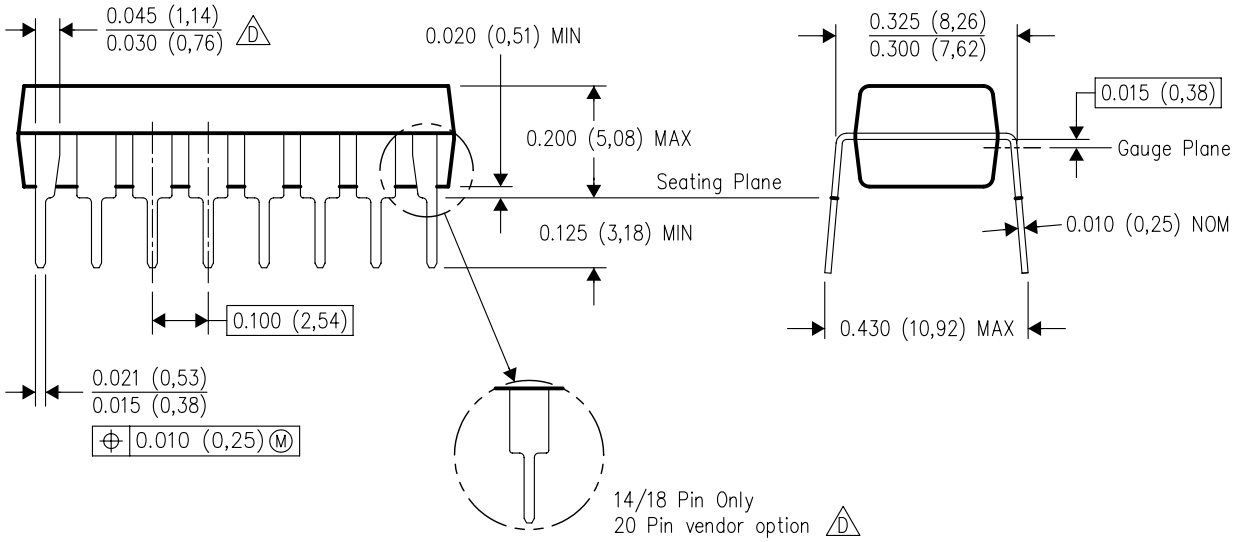
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |

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NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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