on an internal dipole field due to ionisation of DX centre traps in the barriers [1].

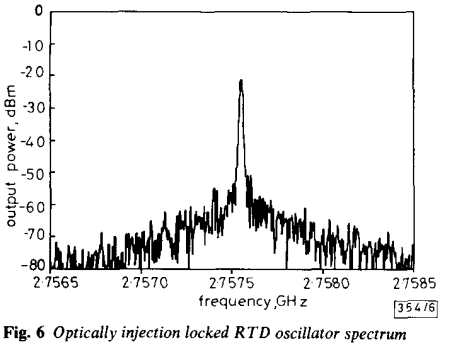

Fig. 6 *Optically injection locked RTD oscillator spectrum*

Conclusion: This Letter has reported preliminary results of direct optical frequency modulation and injection locking of RTD oscillators. It is expected that optimisation of the device structure, oscillator circuit, and optical coupling will result in greater FM sensitivity, larger RF output power, and higher oscillation frequency. Experiments are under way to resolve the optical interaction mechanism.

16th June 1992

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* This work was done while the author held a National Research Council—ETDL Research Associateship

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'STAGGERING SWITCH': AN 'ALMOST-ALL' OPTICAL PACKET SWITCH

Z. Haas

Indexing terms: Optical switching, Delay lines, Optical communication

An 'almost-all' optical packet switch architecture is presented, based on two rearrangeably nonblocking stages interconnected by optical delay lines with different amounts of delay. Probability of loss as a function of link use and the size of the switch is investigated. In general, with proper setting of the number of delay lines, the switch can achieve arbitrarily low probability of loss.

Introduction: The main problem in the implementation of packet-switched optical networks is the lack of optical memory. Some networks cope with this shortcoming by introducing special architectures that either eliminate the need for local buffering or that reduce the size of the buffers [1]. Other networks, especially local area networks, rely on some (electronically-based) reservation scheme that again eliminates the need for optical buffers. However, this approach cannot be easily extended to a wider network span. Therefore, the challenge is to propose an optical switch architecture design with the constraint that large optical storage is not feasible.

Staggering switch architecture: The staggering switch architecture, shown in Fig. 1, is based on two stages: the scheduling stage and the switching stage. Each one of the stages is a

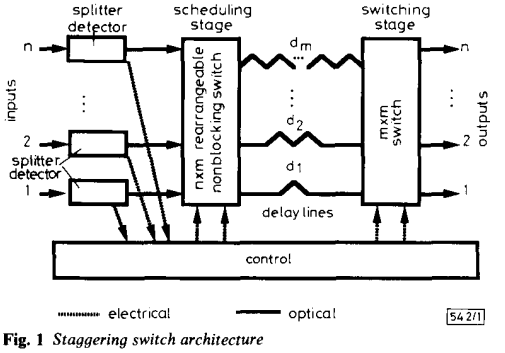

Fig. 1 *Staggering switch architecture*

rearrangeably nonblocking (e.g. Beneš networks with dilation [3]) switching fabric and is implemented with electronically controlled optical devices ($LiNbO_3$, for example). The scheduling stage is $n \times m$ and the switching stage is $m \times n$, where $m \geq n$. The scheduling stage is connected to the switching stage by m delay lines, d_i, $i = 1$ to m. The delay of the d_i delay line equals i packets. Similar hardware was previously used for optical time division switching.

The energy of each one of the n input lines to the switch is split immediately after its arrival; a 'small' fraction of the energy is passed to the detector, converted to an electrical signal, and forwarded to the control section. The control section reads the header bits to determine the required routing for the packet, and drives the scheduling and the switching stages of the switch.

The purpose of the scheduling stage is to distribute the packets arriving on the switch input to the delay lines in such a way that, at any time slot, no two packets arriving at the switching stage are destined for the same output. In other words, the output collisions present in the inputs are resolved by delaying the colliding packets by a different number of slots, so that when they arrive at the switching module, the collisions are resolved.

The control section receives the header information from all the arriving packets and attempts to allocate as many of them as possible into the delay lines, d_i. The scheduling is carried out according to the algorithm presented in the following. Based on the knowledge of the content of the delay lines at any time, the control section can ensure that there are no collisions at the switching stage. Because of the statistical properties of the arrival process, some packets cannot be accommodated (without violating the 'no collisions at the switching stage' principle) and may be lost. The purpose of the switching stage is to permute the outputs of the delay lines, so that the packets emerge at the required switch output.

Fig. 2 gives the definition of a column. In its basic form, the scheduling algorithm is as follows: scanning the inputs sequentially, for each input packet the algorithm tries to insert the packet in the lowest possible delay line, subject to two conditions: that no previous packet was inserted in the delay line in this time slot, i.e. the output is free, and that no other packet to the same destination exists in the column in which the packet is to be inserted. This algorithm gives higher priority to the lower numbered inputs. Other assignments exist which yield different features and performance.

The probability of blockage is defined as the probablity that a randomly chosen packet cannot be scheduled, and is

dropped, P_{block}, and depends on input line use (i.e. the probability that an input slot contains a packet) ρ. It is assumed

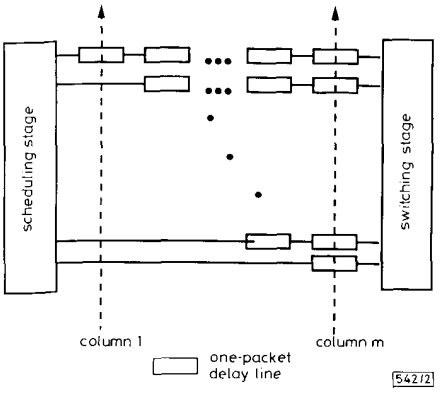

Fig. 2 *Definition of routing algorithm 'data structure'*

that: time is slotted, all the packets are of fixed time duration, the slot size, the arrival of all the packets to the switch, is synchronised, there is no correlation between packets arriving at any two inputs, the distribution of destination numbers on any input is uniform, and there is no correlation between packets arriving on the same input. We will report in the future on the performance when some of these conditions are alleviated.

The probability of blockage is evaluated in Fig. 3 as a function of line use with the size of the switch, n, as a parameter. Thus, for switches of 32 × 32, the P_{block} at $\rho = 0{\cdot}7$ is smaller than 10^{-8}.

An additional parameter is the number of delay lines, m. Increasing m lowers the loss probability. This is shown in Fig. 4, where n is kept constant at 16, and m is varied from 16 to 32. The effect of an increase in m is quite dramatic. For example, at $\rho = 0{\cdot}8$, the P_{block} decreases from $1{\cdot}2 \times 10^{-3}$ to $6 \times \times 10^{-7}$ (i.e. ~3–4 orders of magnitude), when m increased from 16 to 32. Thus, m can serve as a very effective design parameter to achieve a desirable level of performance.

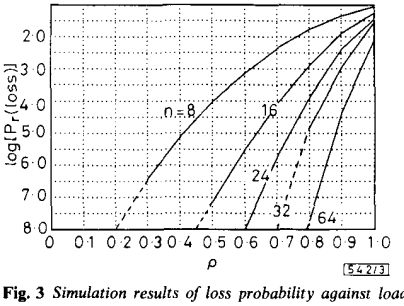

Fig. 3 *Simulation results of loss probability against loading: n = m, n parameter*

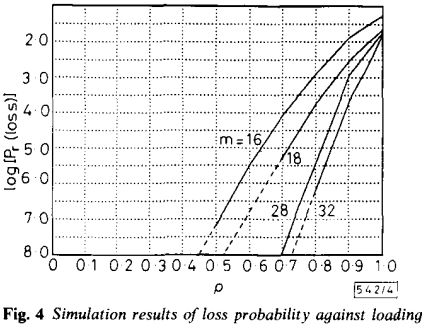

Fig. 4 *Simulation results of loss probability against loading: n = 16, m parameter*

Additional considerations: As discussed in Reference 4, 16 × 16 rearrangeably nonblocking modules were built with an optical power loss of 13·4 dB per module. Thus, connecting two of these modules and accounting for excess losses yields an attenuation of 29 dB. Consequently, if the switch is only one of several switches a packet is going to pass through, some sort of amplification is required.

The staggering switch may resequence packets. A possible solution is to modify the scheduling algorithm, so that loss of packet does not occur. Thus, if a packet arrived on input k to output j and was scheduled on d_i, then the packet arriving on the same input to the same output can be scheduled only on d_h, where $h > i$. In general, if the last packet from input k to output j has arrived s slots ago and was placed on d_i, then a packet from the same input to the same output arriving in the current slot can be placed on d_h, where max $(1, i - s + 1) \leq h \leq m$. This restriction complicated the algorithm and results in larger loss probability. Thus m may need to be larger to achieve the same level of performance. Evaluation of the performance of the order-preserving staggering switch will be reported elsewhere.

Conclusion: We have presented an 'almost-all' optical switch architecture that does not rely on recirculating loops for storage implementation. The architecture is based on two rearrangeably nonblocking stages interconnected by delay lines with different amount of delay. We have estimated that switches 32 × 32 may easily be implemented with the ECL logic.

2nd July 1992

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REDUCING THE NUMBER OF NONZERO ELEMENTS OF TOPOLOGICAL LOOP (B) AND CUTSET (D) MATRICES

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Indexing terms: Matrix algebra, Circuit theory, Networks and network theory

Topological loop (B) and cutset (D) matrices are used to formulate systems of equations in many applications in the symbolic network analysis and fault diagnosis of electronic circuits. The minimisation of the number of their nonzero elements leads to more effective manipulation of the resulting equations. A simple and efficient algorithm for the reduction of the number of these nonzero elements is introduced and some applications are presented showing its effectiveness.

Introduction: The fundamental loop matrix B and the fundamental cutset matrix D of a connected network are often used for the automatic formulation of systems of equations in applications such as computer-aided symbolic network analysis and analogue fault diagnosis [1, 2]. These systems of equations are further manipulated, and a reduced number of nonzero elements (NZEs) certainly leads to more efficient solutions, especially for large circuit graphs.