External Bus to Avalon Bridge

For Quartus II 15.0

1 Core Overview

The External Bus to Avalon Bridge provides a simple interface for a peripheral device to connect with the Avalon® Switch Fabric as a master device. The Bridge creates a bus-like interface to which one or more "master" peripherals can be connected.

2 Functional Description

Figure 1 shows how the External Bus to Avalon Bridge provides a connection between the Avalon Switch Fabric and an external master peripheral.

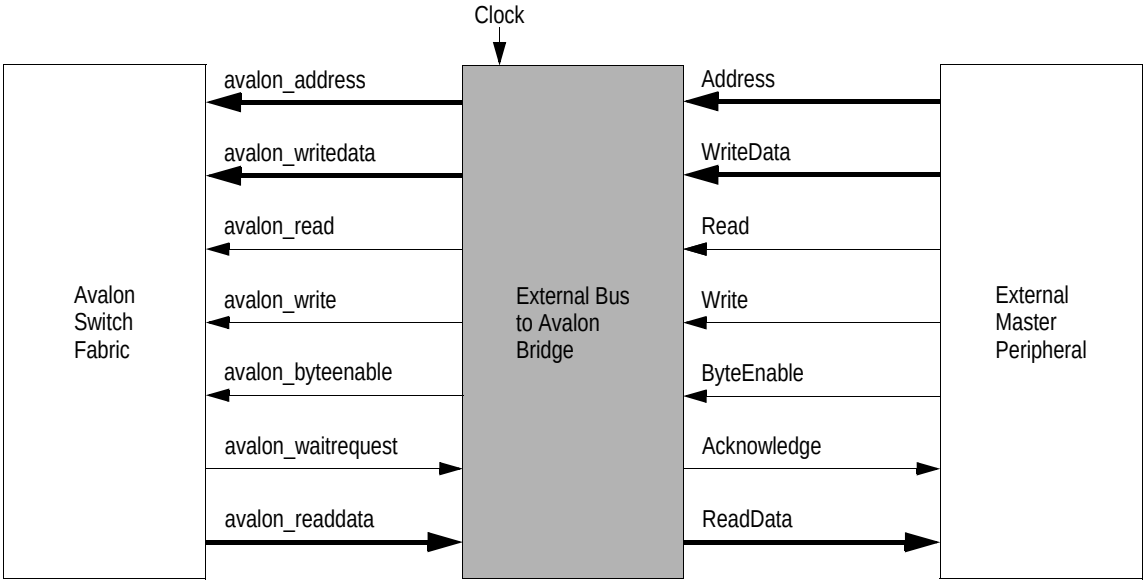

Figure 1. Usage of the External Bus to Avalon Bridge

From the Avalon Switch Fabric's perspective, the External Bus to Avalon Bridge is a master device, because it initiates and controls read/write transfers on the Avalon Switch Fabric. From the external peripheral's perspective, the Bridge is a slave device.

The bus signals provided are:

- Address — *k* bits (up to 32). The address of the data to be transferred. The address is aligned to the data size. For 32-bit data, the address bits $Address_{1-0}$ are equal to 0. The ByteEnable signals can be used to transfer less than 4 bytes.
- Read — 1 bit. Indicates that the data transfer is a Read operation.
- Write — 1 bit. Indicates that the data transfer is a Write operation.
- ByteEnable — 16, 8, 4, 2, or 1 bits. Each bit indicates whether or not the corresponding byte should be read or written. These signals are active high.
- WriteData — 128, 64, 32, 16, or 8 bits. The data to be written to the peripheral device during a Write transfer.
- ReadData — 128, 64, 32, 16 or, 8 bits. The data that is read from the peripheral device during a Read transfer.
- Acknowledge — 1 bit. Used by the peripheral device to indicate that it has completed the data transfer.

The bus is synchronous — all bus signals must be read by the master peripheral on the rising edge of the clock. A bus transfer happens when either Read or Write is high.

Figure 2 shows an example system using the Bridge that connects a Nios® II system implemented on Altera's DE2 Board to a master peripheral.

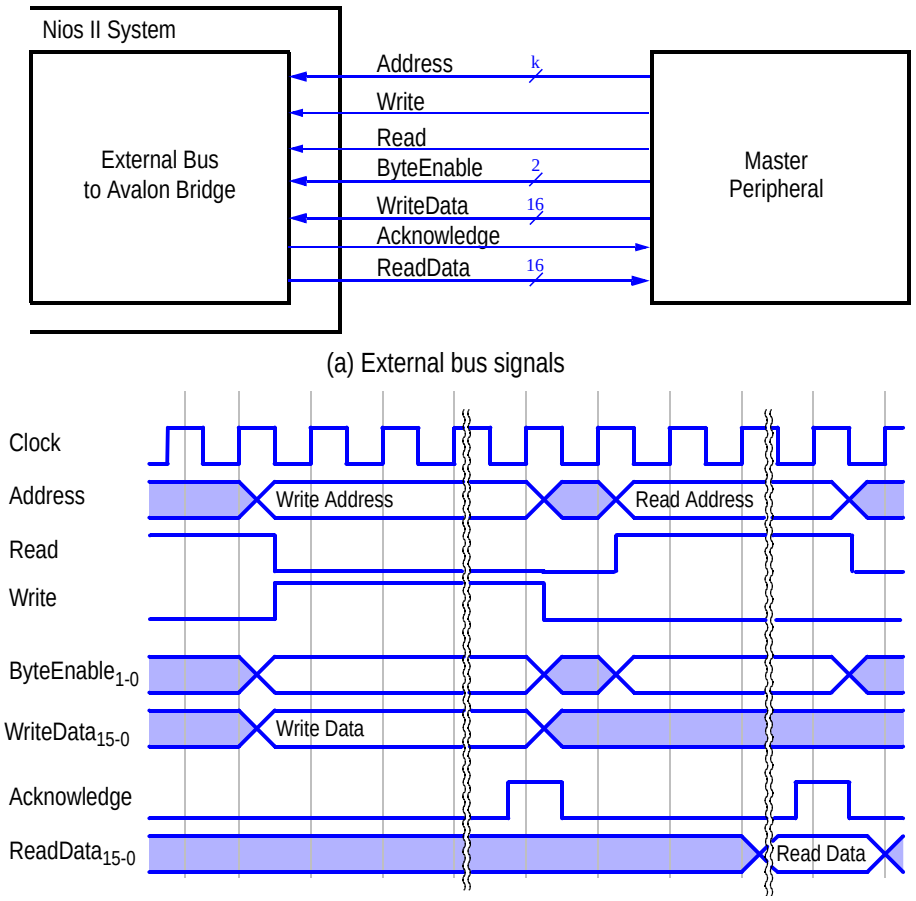

Figure 2. The External to Avalon Bus Bridge signals

3 Instantiating the Core in Qsys

Designers use the External Bus to Avalon Bridge's configuration wizard in Qsys to specify the desired features. Two parameters need to be specified:

Data Width — The number of data bits involved in a transfer. The Bridge supports data widths of 8, 16, 32, 64, and 128 bits.

Address Range — The addressable space supported by the Bridge. It is possible to specify the address range of 1, 2, 4, 8, 16, 32, 64, 128, 256, 512, and 1024, in either bytes, kilobytes (kB) or megabytes (MB).