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Schottky barrier inhomogeneities at the interface of few layer epitaxial graphene and silicon carbide

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In this work, we study electron transport across the heterojunction interface of epitaxial few-layer graphene grown on silicon carbide and the underlying substrate. The observed Schottky barrier is characterized using current-voltage, capacitance-voltage and photocurrent spectroscopy techniques. It is found that the graphene/SiC heterojunction cannot be characterized by a single unique barrier height because of lateral barrier inhomogeneities. A Gaussian distribution of barrier heights with a mean barrier height $\phi_{Bm} = 1.06\,\text{eV}$ and standard deviation $\sigma = 137 \pm 11\,\text{meV}$ explains the experimental data quite well. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4711769]

In recent years, graphene, a two-dimensional honeycomb lattice of carbon atoms, has garnered much attention because of its unique electronic,[1] optical,[2] thermal[3] and mechanical[4] properties. It is imperative to understand the interface between graphene and various metals and semiconductors in order to develop a full picture of the operation of graphene devices. For example, high speed graphene photodetectors have been reported based on photocurrent generated at the graphene-metal interface attributed to local electric fields at the interface.[5] However, recent studies have identified a thermoelectric contribution to the photocurrent,[6] prompting further investigation of the true nature of the origin of photocurrent at the graphene-metal interface. In case of a graphene-semiconductor interface, graphene as a consequence of its zero bandgap, is expected to be analogous to a metal at the contact. Indeed, a Schottky barrier has been reported at the interface between graphene and various semiconductors including Si,[7,8] GaAs,[7] SiC,[7,9–11] and GaN.[12] Because of the rectifying nature of graphene-semiconductor contacts, they could be useful in metal-semiconductor field effect transistors or high electron mobility transistors. Other possible applications include infrared photodetectors and gas sensing.[13]

In this work, we study the Schottky barrier at the interface of few-layer graphene (FLG) grown epitaxially on n-type 4 H-SiC substrates using current-voltage (*I-V*), capacitance-voltage (*C-V*) and photocurrent spectroscopy methods. Barrier heights obtained using the different techniques are compared and examined in the light of lateral barrier inhomogeneities at the junction. We find that a Gaussian distribution of barrier heights with a mean barrier height $\phi_{Bm} = 1.06\,\text{eV}$ and standard deviation $\sigma = 137 \pm 11\,\text{meV}$ explains the experimental data very well.

Si-face of a nitrogen-doped 4° off-axis n^+ 4 H-SiC substrate having a lightly doped n-type epitaxial layer was graphitized by heating at 1400–1500 °C under high vacuum for 1 h. FLG grown on the SiC surface was characterized using a Raman microscope equipped with a 488 nm argon ion laser and spectra were collected in a 180° backscattering geometry. G and 2D peaks corresponding to graphene were seen.[32] A small D peak, indicative of defects in the graphene, was also observed. The D/G peak ratio was in the range of 15%–35%. The FLG was patterned using photolithography and oxygen plasma into circular diode structures with varying diameters from 150–250 μm. 150 nm thick Au was used to contact the FLG. Transfer length method (TLM) structures were also fabricated to measure contact resistance between metal and FLG. 60 nm Ni/100 nm Au was used to make the ohmic back contact to the n^+-SiC substrate. A separate set of control devices with no FLG on the SiC was also fabricated. For these devices, a short 6:1 buffered oxide etch was used to remove any surface oxide. This was followed by evaporation of 150 nm Au to form the diodes.

Electrical measurements were performed using a Desert Cryogenics probe station and an Agilent 4156C Semiconductor Parameter Analyzer. Capacitance measurements were performed using an Agilent 4284A Precision LCR Meter in the frequency range 500 Hz to 1 MHz. Photocurrent experiments were conducted using a supercontinuum source (Fianium SC400-4, total power 4 W, 40 MHz) in the energy range 0.75–1.60 eV. Fig. 1 shows a schematic of the setup. The supercontinuum light was passed through a double-pass monochromator to produce a source with linewidth 40 nm. A calibrated glass coverslip served as a beam splitter, enabling simultaneous measurement of the short circuit photocurrent at the sample and the incident photon intensity. Optical power was measured using a Si or InGaAs power/wave head. Removal of the gold top contact from portions of the Schottky device enabled light to be incident from the FLG-side of the sample. Photocurrent was measured using lock-in detection at 41 Hz.

Fig. 2(a) shows *I-V* characteristics of a TLM device with 2 μm separation between the pads over a temperature range 4.2 K–298 K. The curves are linear with little change in slope, suggesting that the transport is primarily occurring through the pathway Au/FLG/Au. Thus, we conclude that the Au/FLG interface is non-rectifying. Fig. 2(b) displays a typical plot of resistance vs pad spacing for Au/FLG devices

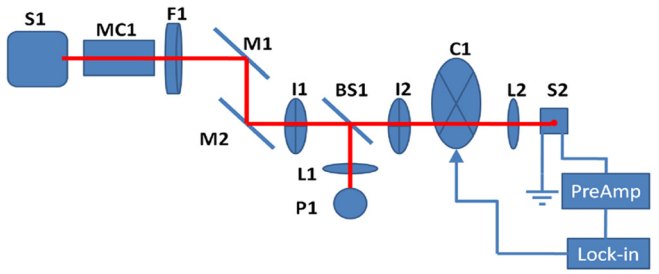

FIG. 1. Setup of the photocurrent spectroscopy experiment. Path of the light beam is shown in red. Light is incident on the junction from the FLG side.

at 4.2 K. A sheet resistance $R_s = 1.1$ kΩ/□ and a contact resistance $R_c = 11\Omega$ were extracted from the plot for $200 \times 200\ \mu m^2$ contact pads.

I-V measurements of Au/FLG/SiC devices exhibit rectifying behavior. Forward *I-V* characteristics for a typical device (150 μm diameter) are shown in Fig. 3(a) over the temperature range 250 K–375 K. Measurements at lower temperatures were unreliable because of freeze-out effects in the SiC.[14] Since the Au/FLG interface is Ohmic, the rectification must arise from the FLG/SiC interface. Fig. 3(b) is a plot of the diode capacitance as a function of reverse bias voltage at

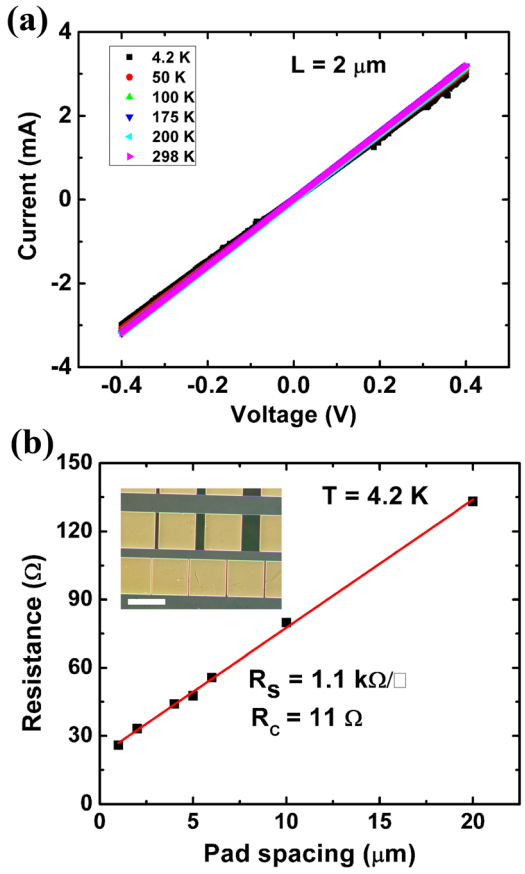

FIG. 2. (a) *I-V* characteristics of a 2 μm Au/FLG/Au TLM structure over the temperature range 4.2 K–298 K. (b) TLM plot of resistance as a function of pad spacing at 4.2 K. Linear fit is shown using solid line. Inset shows microscope image of the TLM structure. The darker regions, where graphene is present, are still covered with photoresist. Scale bar is 200 μm.

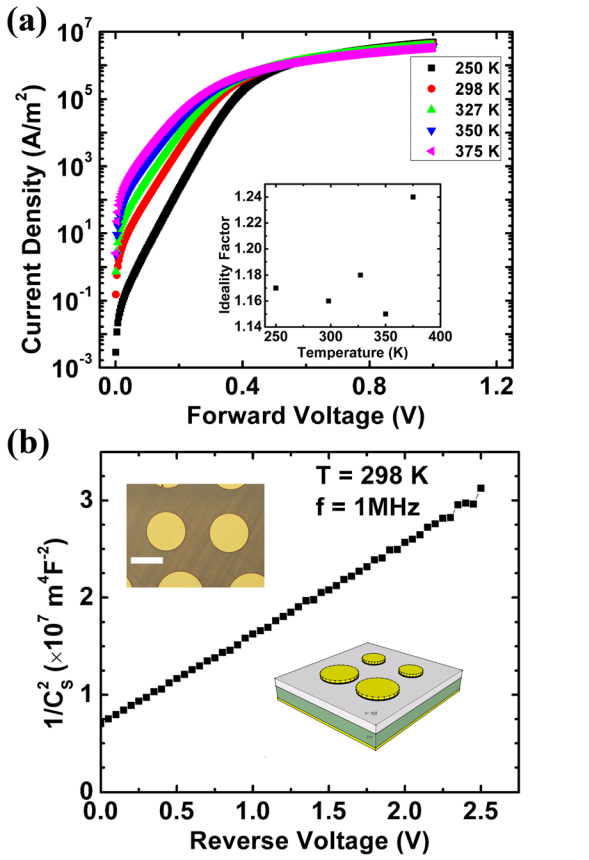

FIG. 3. (a) Forward *J-V* characteristics of a 150 μm diameter FLG/SiC diode over the temperature range 250 K–375 K. Inset shows ideality factor vs temperature. (b) Plot of the diode capacitance per unit area as a function of reverse bias voltage at 1 MHz and 298 K. Insets show an optical microscope image and a schematic figure of the diodes. Scale bar is 200 μm.

1 MHz and 298 K. Similar measurements were performed on Au/SiC control samples with no graphene at the interface.

According to the thermionic emission model, the current, *I*, for a voltage drop, $V \gg \frac{k_B T}{q}$, across the diode at temperature *T* may be expressed as[15]

$$\mathrm{I} = I_0 e^{\frac{qV}{nk_B T}}. \tag{1}$$

The pre-factor $\mathrm{I}_0 = SA^{**}T^2 e^{-\frac{q\phi_{E0}}{k_B T}}$ is the saturation current, where *S* is the area of the diode, A^{**} is the modified Richardson constant of the semiconductor, and ϕ_{E0} is the effective barrier height at zero bias and *n* is the ideality factor. From the linear portion of the I-V characteristics at large forward bias, we obtain an estimate for the series resistance in our devices to lie between 6–11 Ω over the entire temperature range. In subsequent analysis, we only consider the portion of the forward bias with $V_A < 0.3$, where the effect of series resistance can be neglected. Using the known values of the diode area *S* and the theoretical value of 4H-SiC Richardson constant $A^{**} = 146$ A cm^{-2} K^{-2},[16] the barrier height ϕ_{E0} may be obtained from *I-V* data.

The capacitance per unit area, C_S, of a Schottky diode under reverse bias *V* is given by the depletion capacitance[15]

$$C_S = \left(\frac{q\epsilon_s N_D}{2}\right)^{\frac{1}{2}} \left(V + \frac{\phi_{BC} - \xi - k_B T}{q}\right)^{-\frac{1}{2}}, \tag{2}$$

where ϵ_s is the permittivity of the semiconductor (for 4 H-SiC, $\epsilon_s = 9.87\epsilon_0$), N_D is the doping density, ϕ_{BC} is the barrier

height, and ξ is the distance of the Fermi level below the conduction band in the charge-neutral semiconductor at equilibrium. From a plot $1/C^2$ vs V, one can deduce the barrier height ϕ_{BC} and the doping in the semiconductor. The results of analyses using Eqs. (1) and (2) for 12 FLG/SiC and 3 Au/SiC devices at 298 K are presented in Table I. The doping density of the n-SiC layer from the slope of the $1/C_S^2 - V$ plot is $(1.9\pm0.1) \times 10^{16}\text{cm}^{-3}$, which agrees well with the specified doping $2 \times 10^{16}\text{cm}^{-3}$.

Table I shows that Au/SiC diodes have low ideality factors. In addition, the barrier heights from *I-V* and *C-V* measurements are comparable. As an example from literature, barrier heights measured on Au/4H-SiC diodes using *I-V* and *C-V* methods were reported to be 1.73 and 1.80 eV, respectively.[16] The small discrepancy between ϕ_{E0} and ϕ_{BC} can be explained as a consequence of the $n > 1$ ideality factor which leads to a difference between the flat-band barrier height measured by the *C-V* method and the zero-bias barrier height measured by the *I-V* method. The barrier heights satisfy the relationship $\phi_{BC} = n\phi_{E0} - (n-1)\left(\xi + \frac{k_BT}{q}\right)$ which was derived in Ref. 17 for non-ideal Schottky contacts.

FLG/SiC diodes exhibit a slightly larger ideality factor, but are comparable to reports in literature.[9] However, a much bigger discrepancy between ϕ_{E0} and ϕ_{BC} exists. Unlike above, this cannot be explained as a consequence of non-ideality. The difference was found to persist over the entire temperature range. Such differences have been reported before in previous works examining the FLG/SiC interface[7,9] but have not been studied. In the rest of the paper, we investigate the reasons for this discrepancy.

Various models were explored in order to explain the observations. The *C-V* data show little dispersion in the frequency range 500 Hz–1 MHz. This rules out effects due to deep traps in the SiC. Because of the wide bandgap of 4H-SiC viz. 3.23 eV and low doping of the epitaxial layer, we do not expect to have significant contributions from image force lowering, recombination in the depletion region, and field/thermionic-field emission effects.[15] This leaves three possibilities to be considered: (a) presence of an interfacial layer with interface states, (b) sheet resistance of graphene, and (c) barrier inhomogeneities. Though it is likely that interface states are the reason for $n > 1$ in the forward bias, interfacial layer models[18] were inadequate to explain the large difference between *I-V* and *C-V* barrier heights. Sheet resistance of the FLG could also lead to overestimation of the barrier height from *C-V* measurements.[19] However, the measured sheet resistance of FLG was not high enough to account for the discrepancy.

This leads us to consider the possibility of a laterally inhomogeneous barrier. A Gaussian distribution of barrier heights has been proposed on other Schottky barrier systems to explain differences in the barrier heights from current and capacitance measurements (see e.g., Ref. 20 and references therein). Two of the earliest works which develop an analytical theory for electron transport by thermionic emission in case of a Gaussian distribution of barrier heights are by Werner and Güttler[21] and Tung.[22]. According to the model, the Schottky barrier is composed of patches with a distribution of barrier heights over a length scale smaller than, or comparable to, the depletion region width. The expression for current through such a junction for $V \gg \frac{k_BT}{q}$ takes the form

$$I = SA^{**}T^2 e^{-\frac{q\phi_E}{k_BT}} e^{\frac{qV}{nk_BT}}. \tag{3}$$

All symbols have the same meanings as before. ϕ_E is the effective barrier height extracted from *I-V* measurements. The *C-V* technique, on the other hand, measures the mean barrier height ϕ_{Bm} of the inhomogeneous junction. The relationship between the two is given by

$$\phi_E = \phi_{Bm} - \frac{q\sigma^2}{2k_BT}, \tag{4}$$

where σ is the standard deviation of the Gaussian distribution. Assuming that σ is temperature-independent, Eq. (4) suggests that a plot of the difference between the barrier heights measured by *C-V* and *I-V* techniques vs $1/T$ should yield an estimate for the spread of the distribution.[21,23] Such a plot is

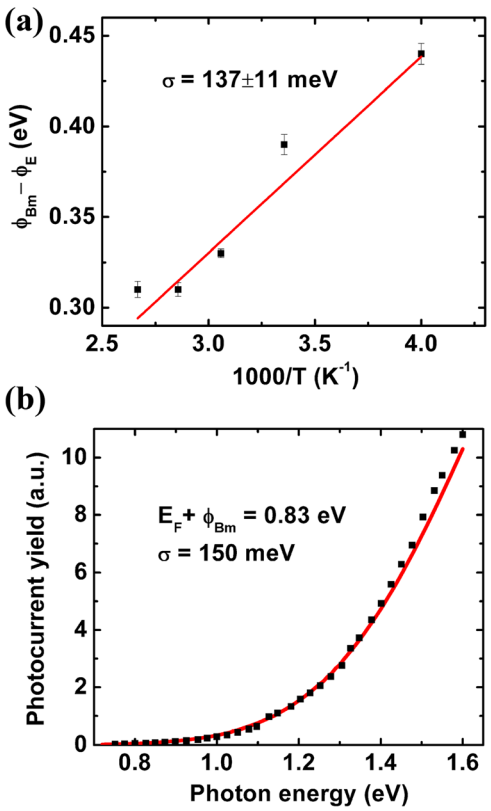

FIG. 4. (a) Plot of the difference between the *C-V* and *I-V* barrier heights as a function of $1/T$. Linear fit is shown by solid line. (b) Photocurrent yield plotted as a function of photon energy at 298 K. Shown with solid line is a fit using a model which explains the observed photocurrent as an internal photoemission process from FLG to SiC across an inhomogeneous barrier with a Gaussian distribution of barrier heights. Parameters from the fit are shown.

TABLE I. Table showing average parameters for 12 FLG/SiC and 3 Au/SiC devices at 298 K. *C-V* measurements were performed at 1 MHz.

Device	n	ϕ_{E0} (eV)	ϕ_{BC} (eV)
FLG/SiC	1.15 ± 0.04	0.67 ± 0.06	1.06 ± 0.12
Au/SiC	1.07 ± 0.01	1.58 ± 0.07	1.68 ± 0.06

shown in Fig. 4(a), from which we compute $\sigma = 137 \pm 11$ meV. A previous work[11] studying the FLG/SiC interface over sub-micron dimensions using a scanning current probe method found a similar Gaussian distribution of barrier heights, with the spread being 100 meV. This lends support to our explanation based on lateral barrier inhomogeneities.

Further evidence for barrier inhomogeneities is presented by photocurrent measurements. Fig. 4(b) shows a plot of the photocurrent yield at the FLG/SiC interface vs incident photon energy. The data is modeled assuming an internal photoemission process from graphene into the SiC.[32] A Gaussian distribution of barrier heights is found necessary to fit the data. We are able to extract a value for the parameter $E_F + \phi_{Bm} = 0.83$ eV from a fit to the photocurrent data, where E_F is the separation of the Fermi level in graphene from the Dirac point. In addition, the value for σ from the fit is 150 meV, which agrees satisfactorily with the earlier estimate from electrical measurements. For the mean barrier height ϕ_{Bm} from photocurrent and C-V measurements to agree, the Fermi level should lie 0.24 ± 0.12 eV below the Dirac point. This suggests an average p-doping of the graphene layer, which has been observed in experiments conducted by other groups.[24–26]

Finally, we speculate on the origin of the inhomogeneous barrier at the FLG/SiC interface. It is known that the local barrier at a metal-semiconductor interface is highly dependent on the interfacial structure. Possible reasons for variation in the barrier height include dislocations, grain boundaries, and structure-dependent interface dipoles.[21,27] Recently, TEM studies have shown that graphene grown over terrace step edges on the SiC contain a high density of structural defects.[28] The substrates used in this study had a 4° miscut with respect to the c-axis. Thus, we expect a lot of step edges in our devices, the dimensions of which are of the order of several hundred microns. STM studies have also shown existence of hexagon-pentagon-heptagon defects in the interface layer.[29] Such defects could contribute to the observed inhomogeneity. In addition, doping domains in graphene[30,31] could shift the Fermi level and cause variations in the Schottky barrier height. The microscopic nature of the origin of the inhomogeneities requires additional study and is beyond the scope of this work.

In summary, the Schottky barrier at the interface of FLG/SiC was studied using a combination of electrical and photocurrent measurements. The results can be explained as a consequence of barrier inhomogeneities at the FLG/SiC interface, which may be a consequence of structural imperfections or doping domains. In order to be useful for applications, it is necessary to be able to control the barrier height precisely. Possible ways to achieve such improvement might involve making devices on a single terrace without crossing a terrace step edge or investigating growth conditions which can lead to formation of FLG with minimum compressive stress and defects.[29]

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[32]See Supplementary material at http://dx.doi.org/10.1063/1.4711769 for an example Raman spectrum and for details of the photocurrent model.