

## **AN-31 Op Amp Circuit Collection**

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### **ABSTRACT**

This application report provides basic circuits of the Texas Instruments op amp collection.

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## 1 Introduction

Texas Instruments recommends replacing 2N2920 and 2N3728 matched pairs with LM394 in all application circuits.

## 2 Basic Circuits

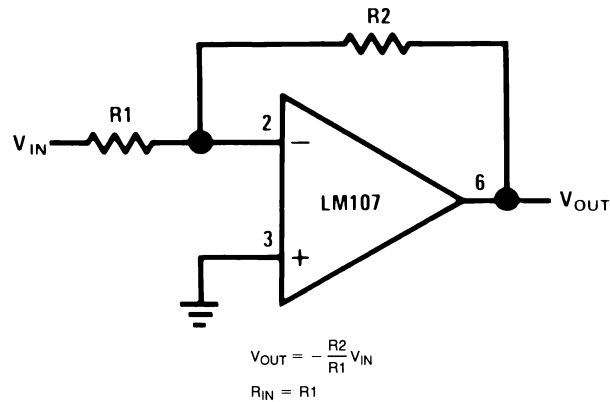


Figure 1. Inverting Amplifier

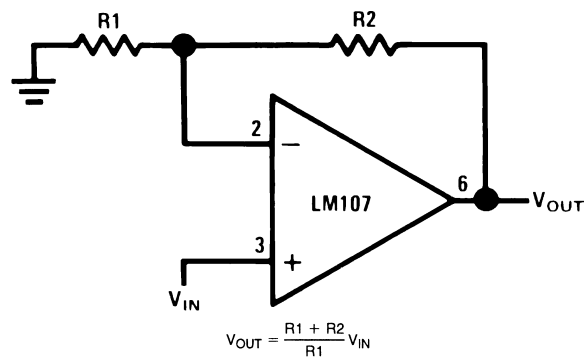
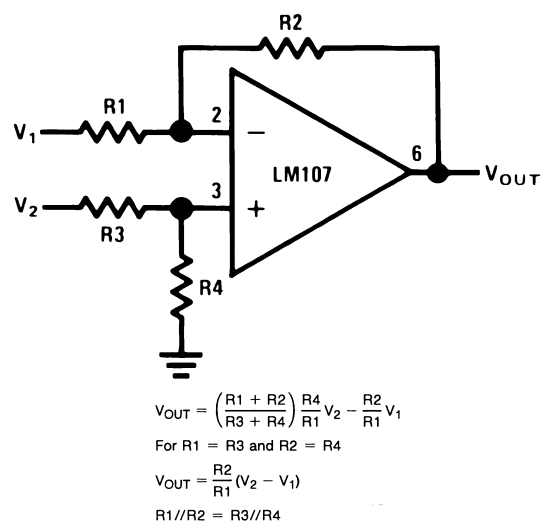
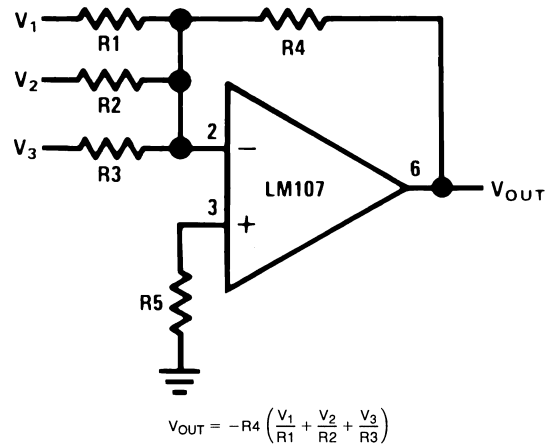


Figure 2. Non-Inverting Amplifier



For minimum offset error due to input bias current.

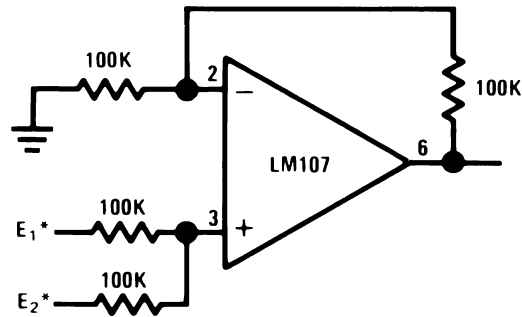
Figure 3. Difference Amplifier



$R5 = R1 // R2 // R3 // R4$

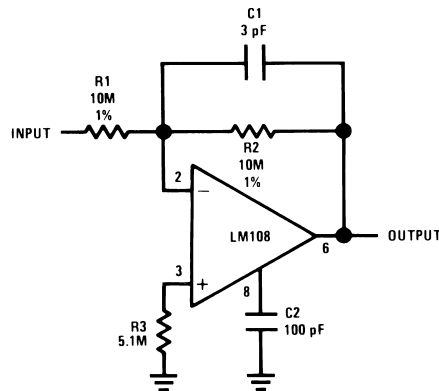
For minimum offset error due to input bias current/

**Figure 4. Inverting Summing Amplifier**



\*  $R_S = 1k$  for 1% accuracy

**Figure 5. Non-Inverting Summing Amplifier**



\* Source Impedance less than 100k gives less than 1% gain error.

**Figure 6. Inverting Amplifier with High Input Impedance**

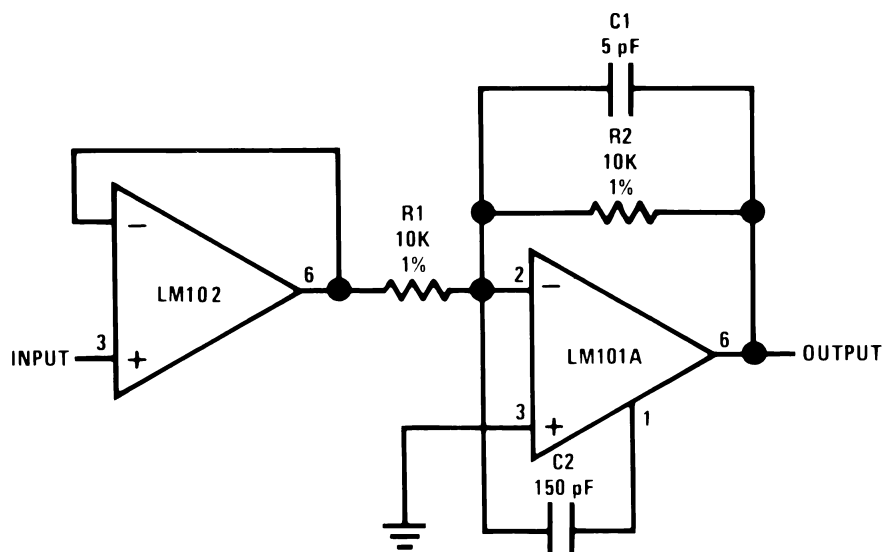


Figure 7. Fast Inverting Amplifier with High Input Impedance

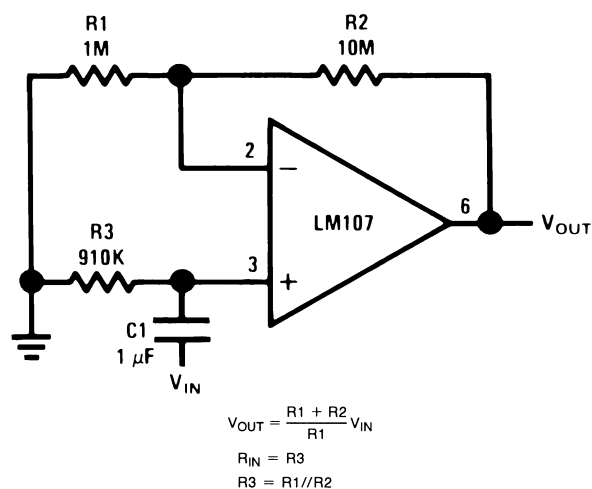


Figure 8. Non-Inverting AC Amplifier

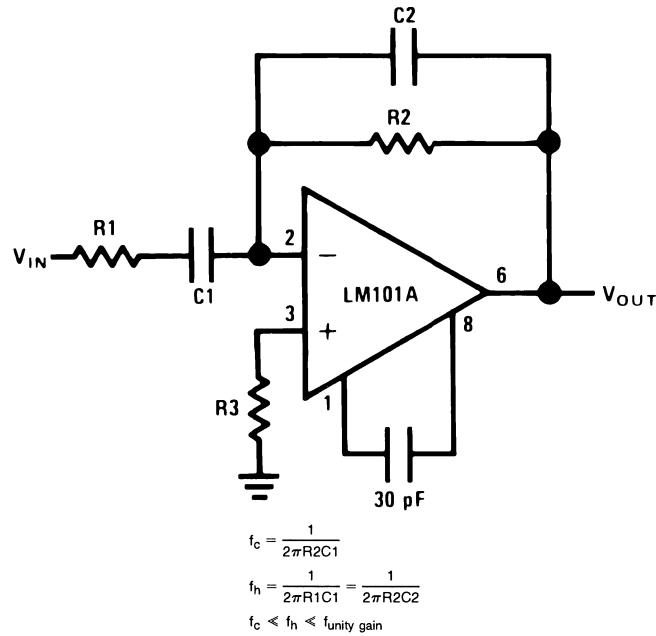
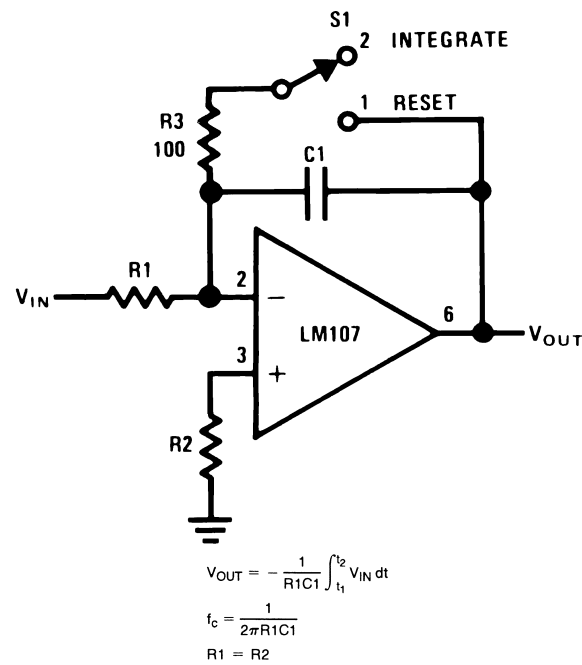


Figure 9. Practical Differentiator



For minimum offset error due to input bias current.

Figure 10. Integrator

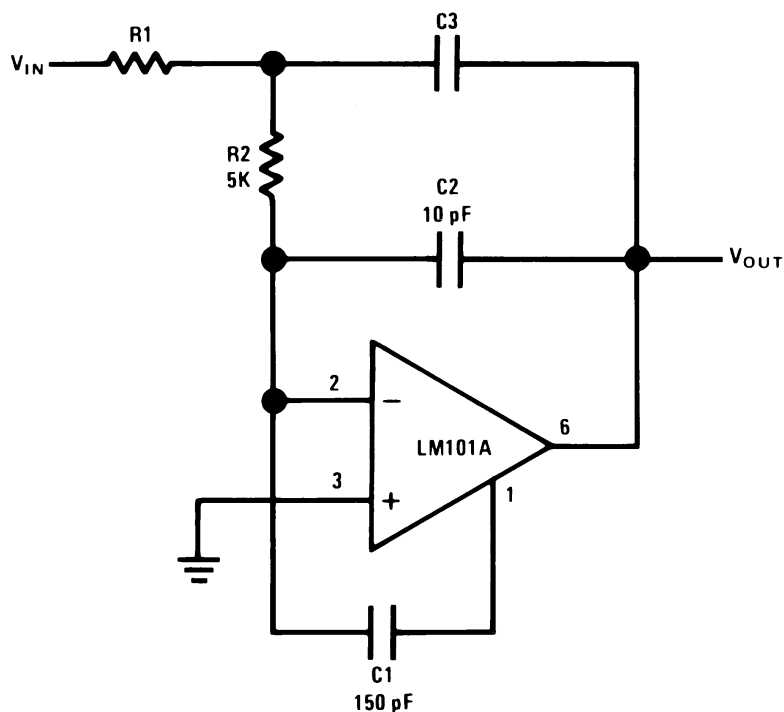
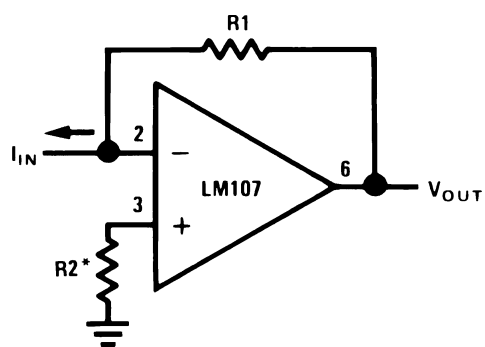


Figure 11. Fast Integrator



$$V_{OUT} = I_{IN} R1$$

\*For minimum error due to bias current  $R2 = R1$

Figure 12. Current to Voltage Converter



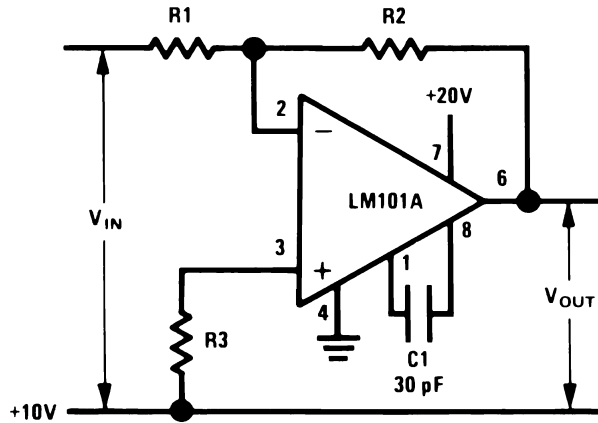


Figure 13. Circuit for Operating the LM101 Without a Negative Supply

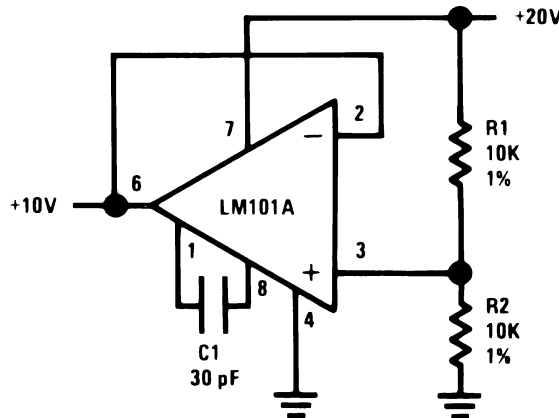


Figure 14. Circuit for Generating the Second Positive Voltage

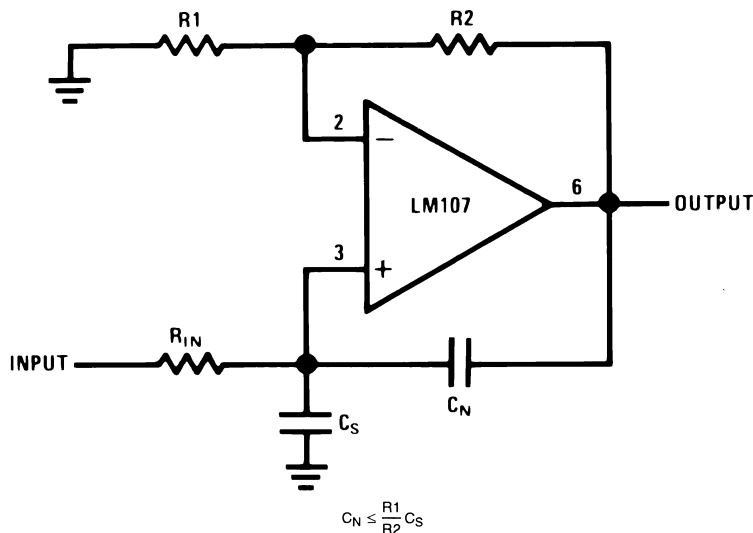
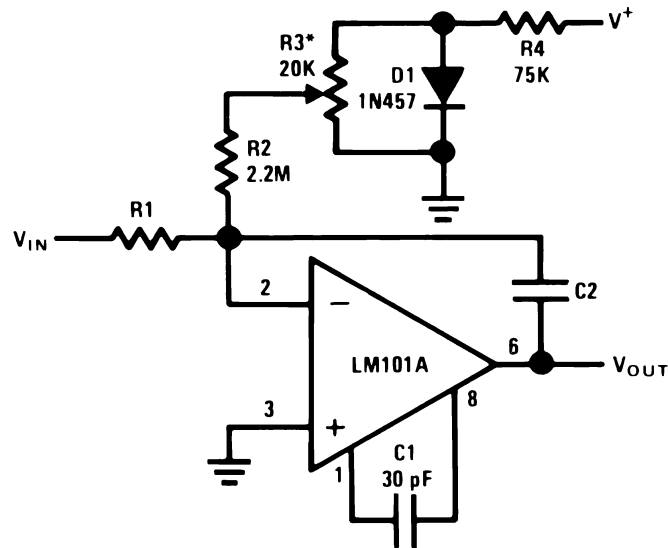
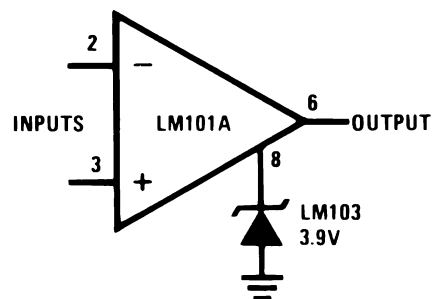


Figure 15. Neutralizing Input Capacitance to Optimize Response Time



\* Adjust for zero integrator drift.  
Current drift typically 0.1 nA/°C over -55°C to 125°C temperature range.

**Figure 16. Integrator with Bias Current Compensation**



**Figure 17. Voltage Comparator for Driving DTL or TTL Integrated Circuits**

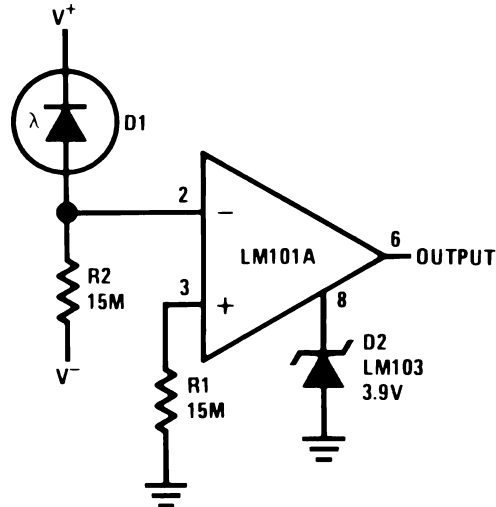
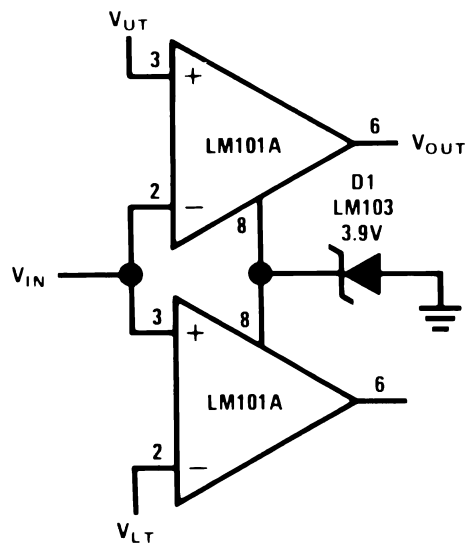


Figure 18. Threshold Detector for Photodiodes



$$V_{OUT} = 4.6V \text{ for } V_{LT} \leq V_{IN} \leq V_{UT}$$

$$V_{OUT} = 0V \text{ for } V_{IN} < V_{LT} \text{ or } V_{IN} > V_{UT}$$

Figure 19. Double-Ended Limit Detector

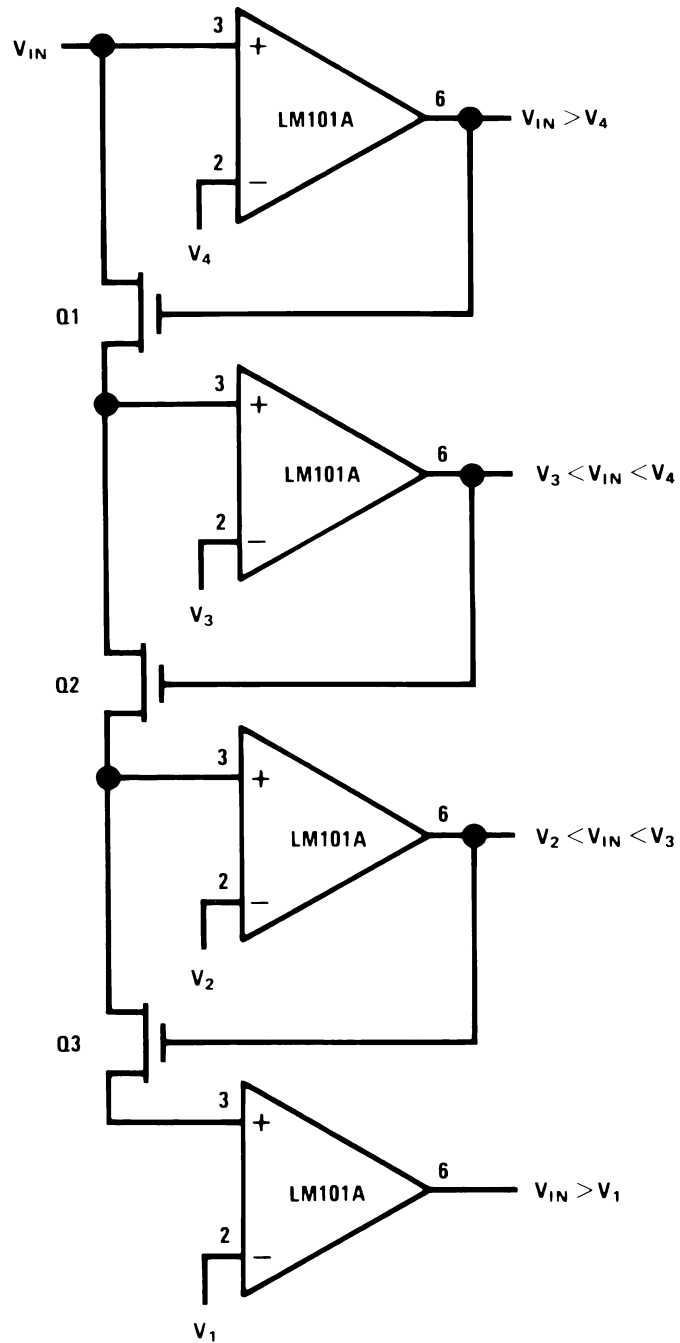


Figure 20. Multiple Aperture Window Discriminator

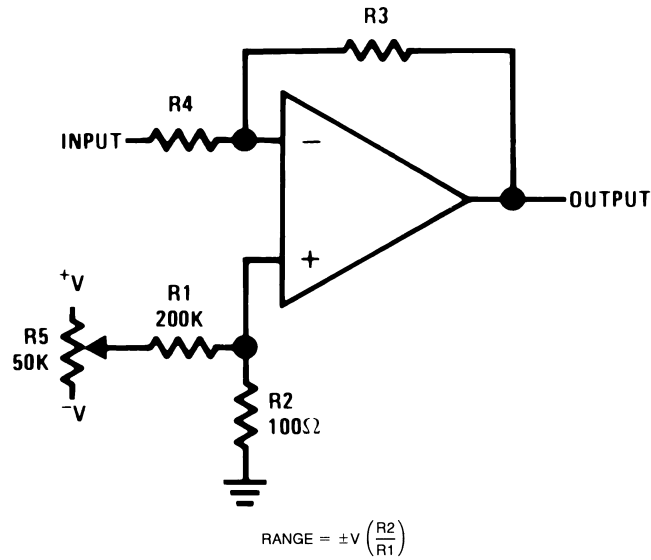


Figure 21. Offset Voltage Adjustment for Inverting Amplifiers Using Any Type of Feedback Element

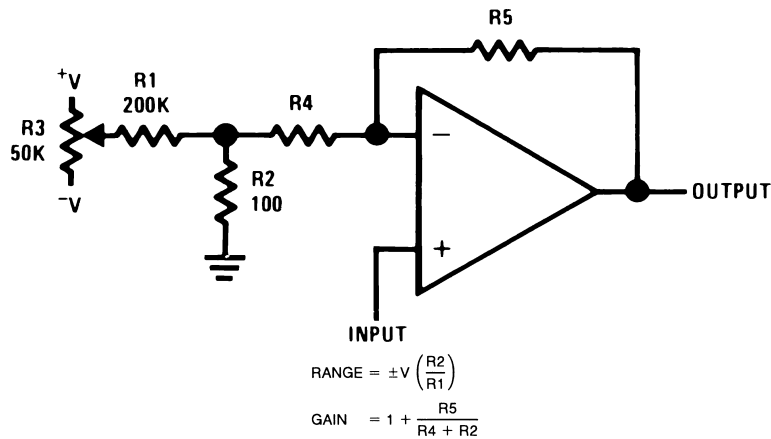


Figure 22. Offset Voltage Adjustment for Non-Inverting Amplifiers Using Any Type of Feedback Element

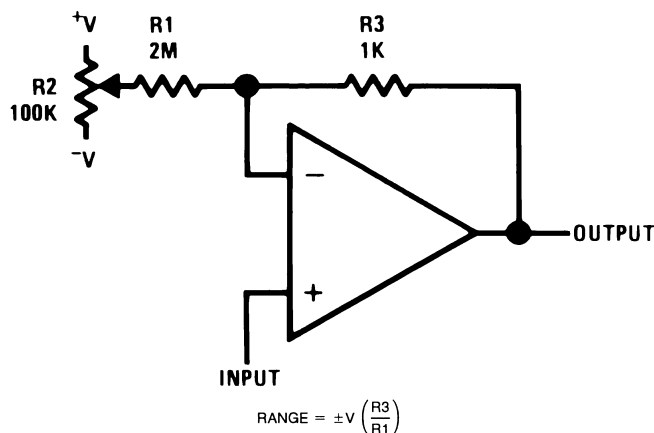


Figure 23. Offset Voltage Adjustment for Voltage Followers

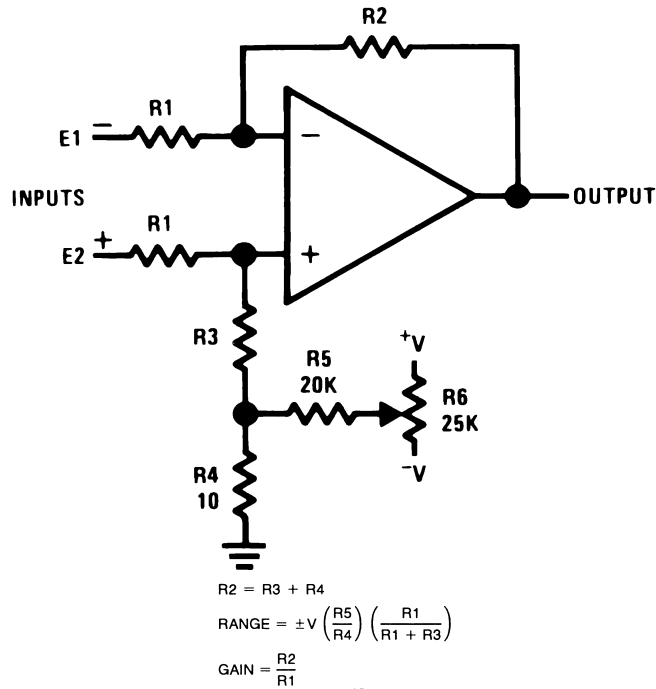


Figure 24. Offset Voltage Adjustment for Differential Amplifiers

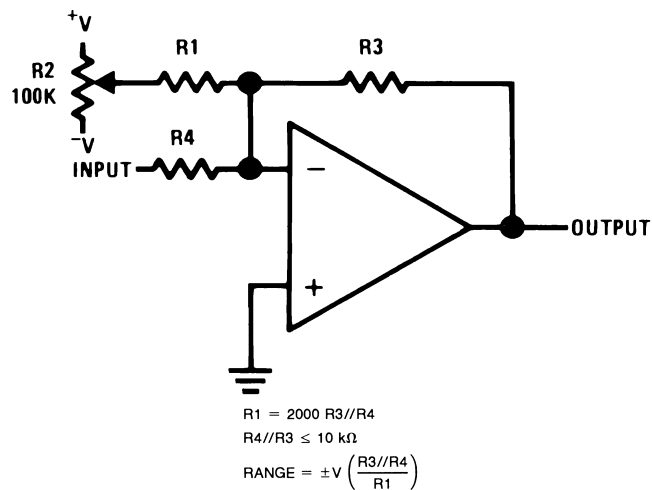


Figure 25. Offset Voltage Adjustment for Inverting Amplifiers Using 10 kΩ Source Resistance or Less

3 Signal Generation

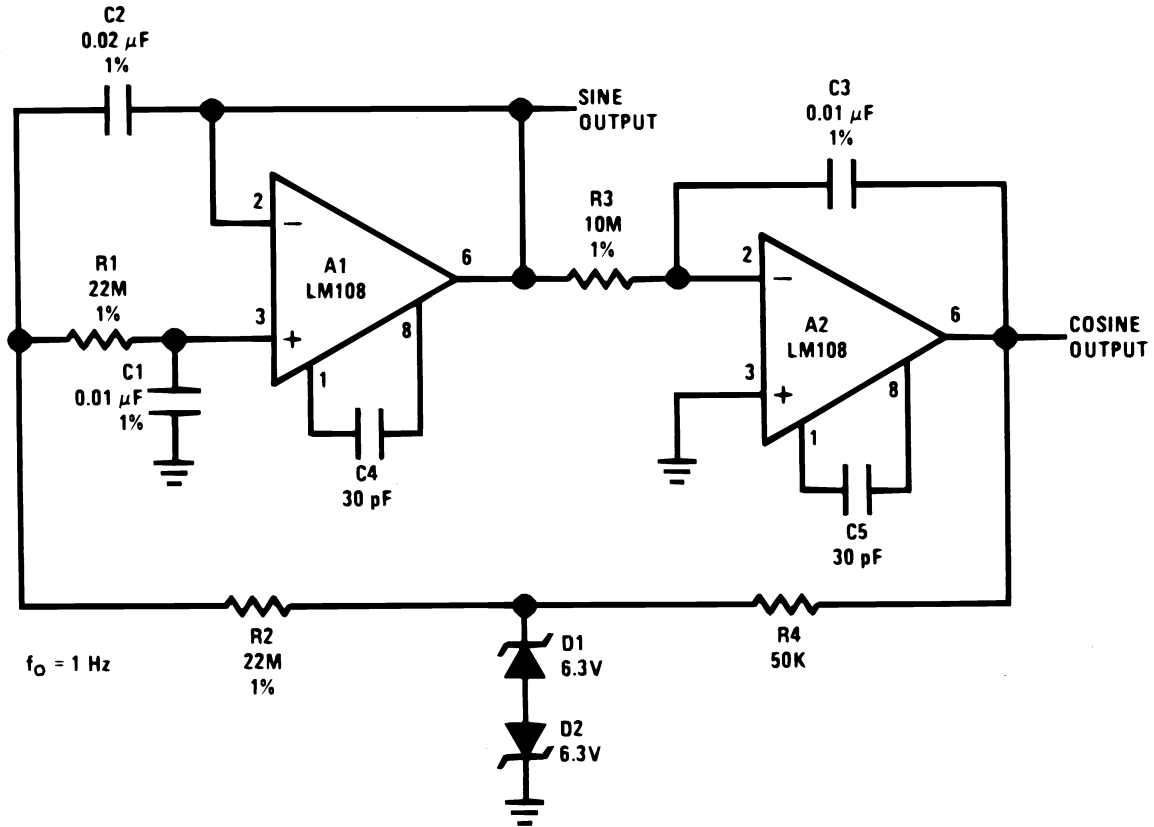


Figure 26. Low Frequency Sine Wave Generator with Quadrature Output

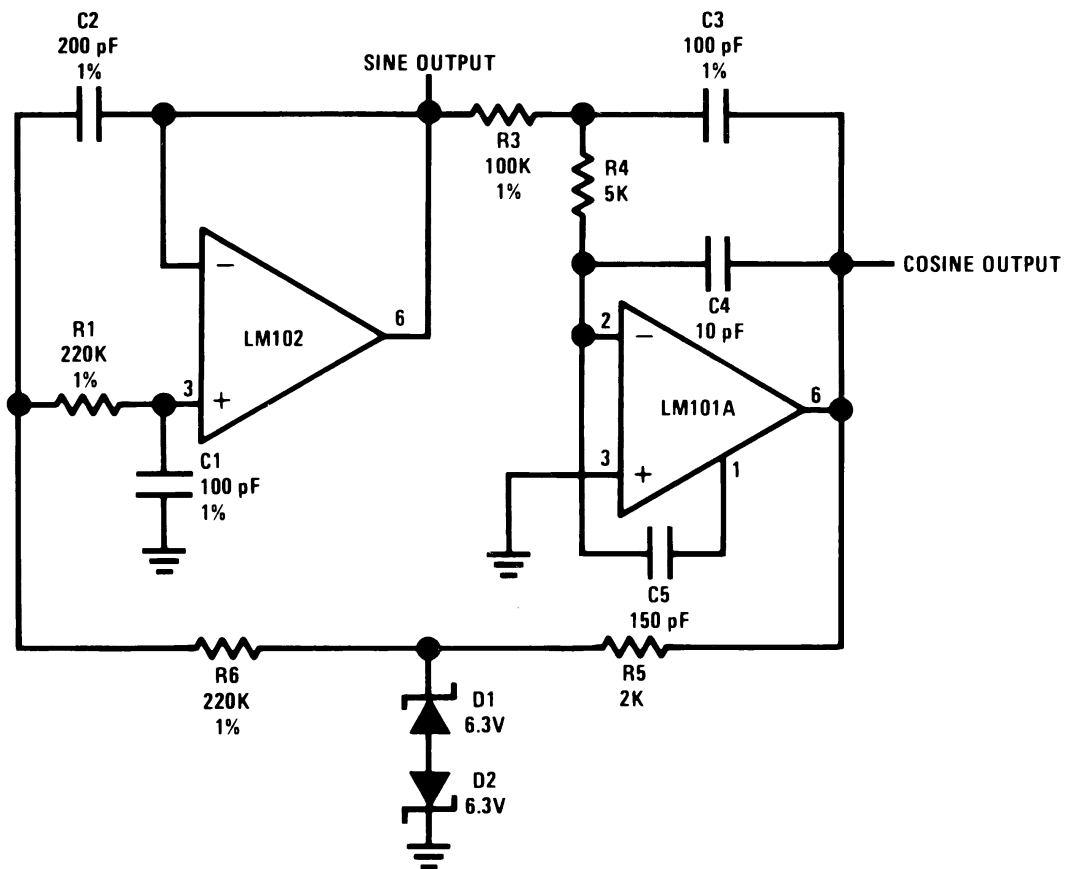
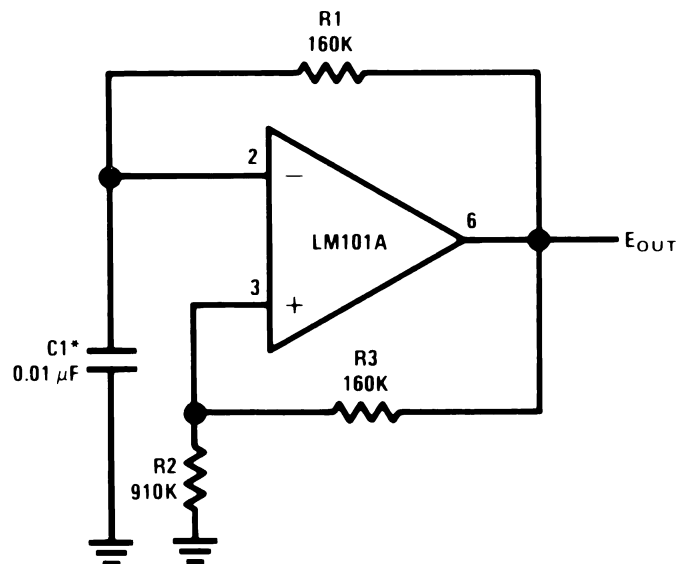


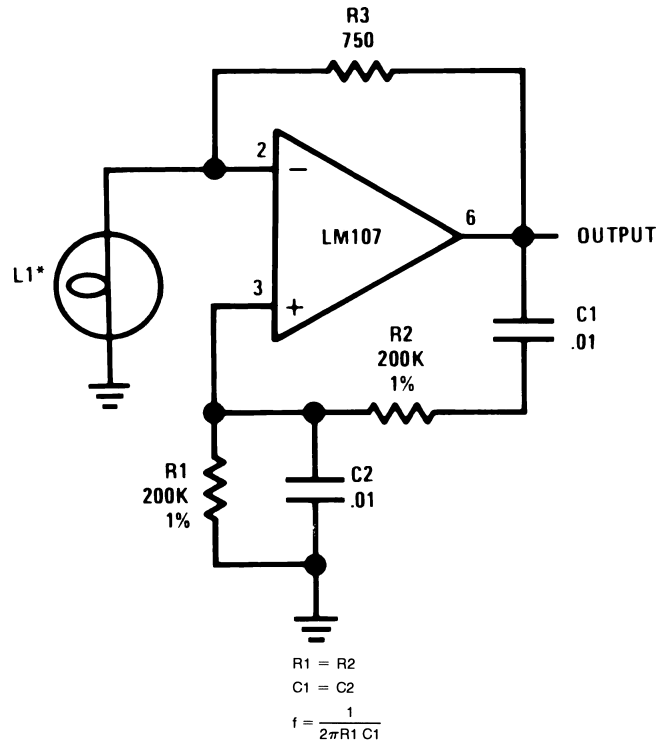
Figure 27. High Frequency Sine Wave Generator with Quadrature Output



\* Chosen for oscillation at 100 Hz

Figure 28. Free-Running Multivibrator





\* Eldema 1869 10V, 14 mA Bulb

Figure 29. Wein Bridge Sine Wave Oscillator

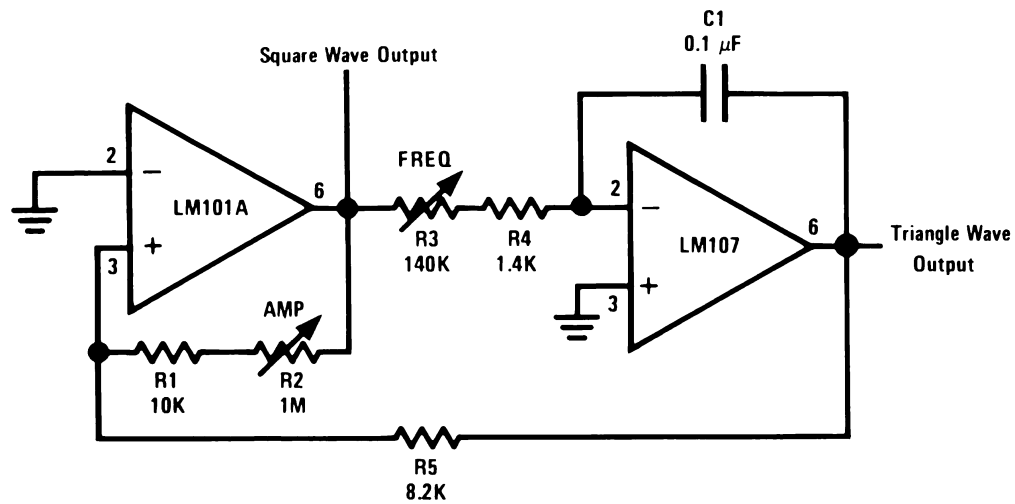


Figure 30. Function Generator

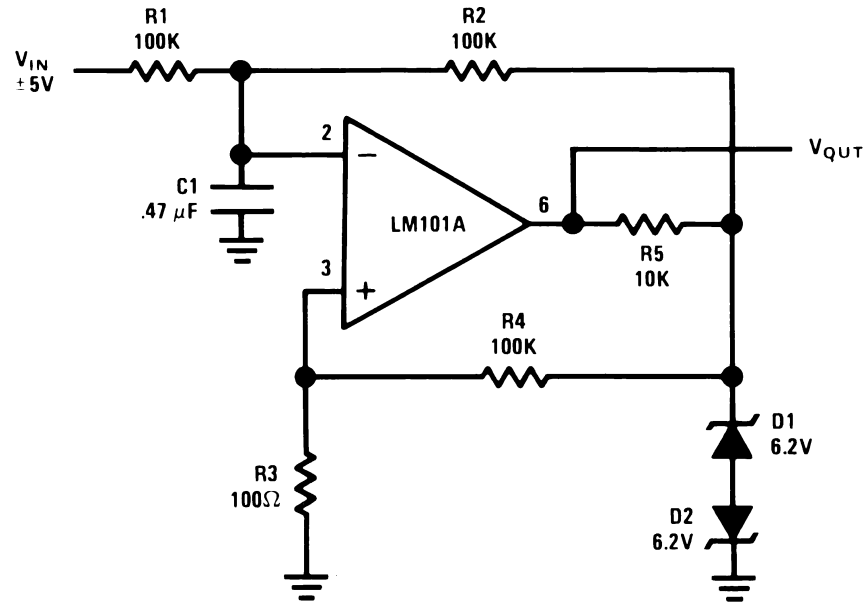


Figure 31. Pulse Width Modulator

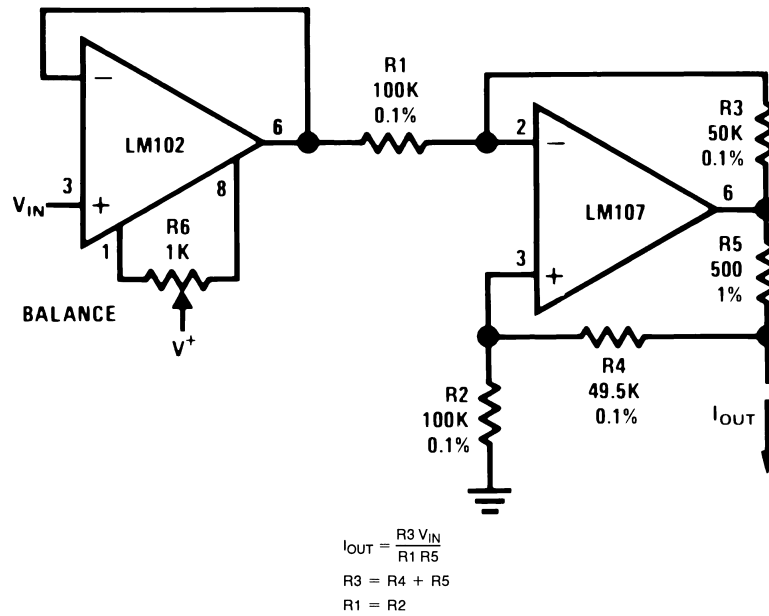


Figure 32. Bilateral Current Source

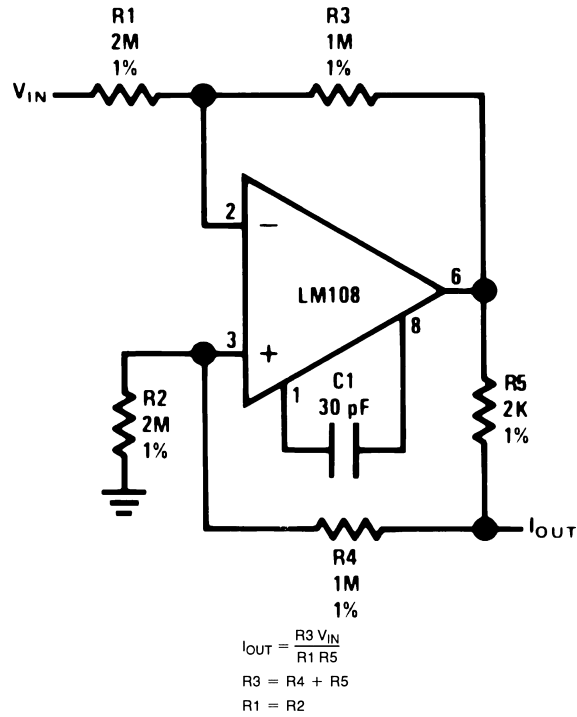


Figure 33. Bilateral Current Source

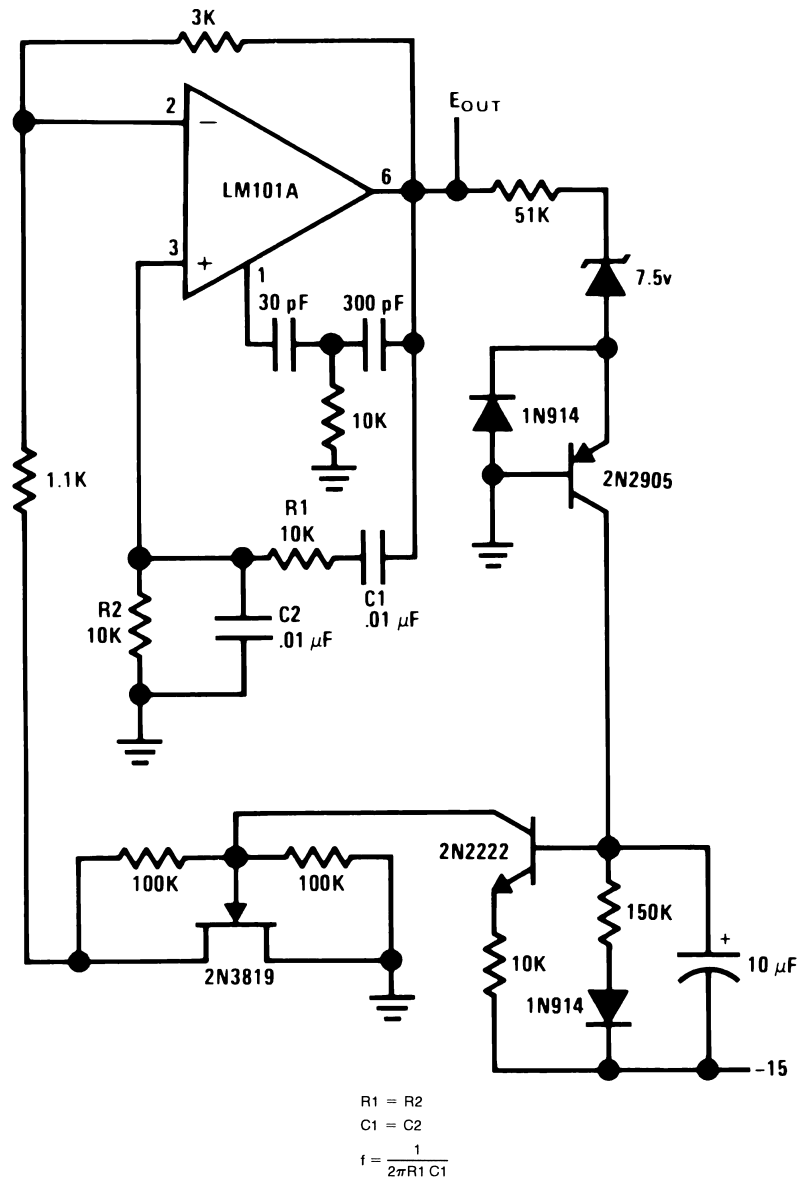
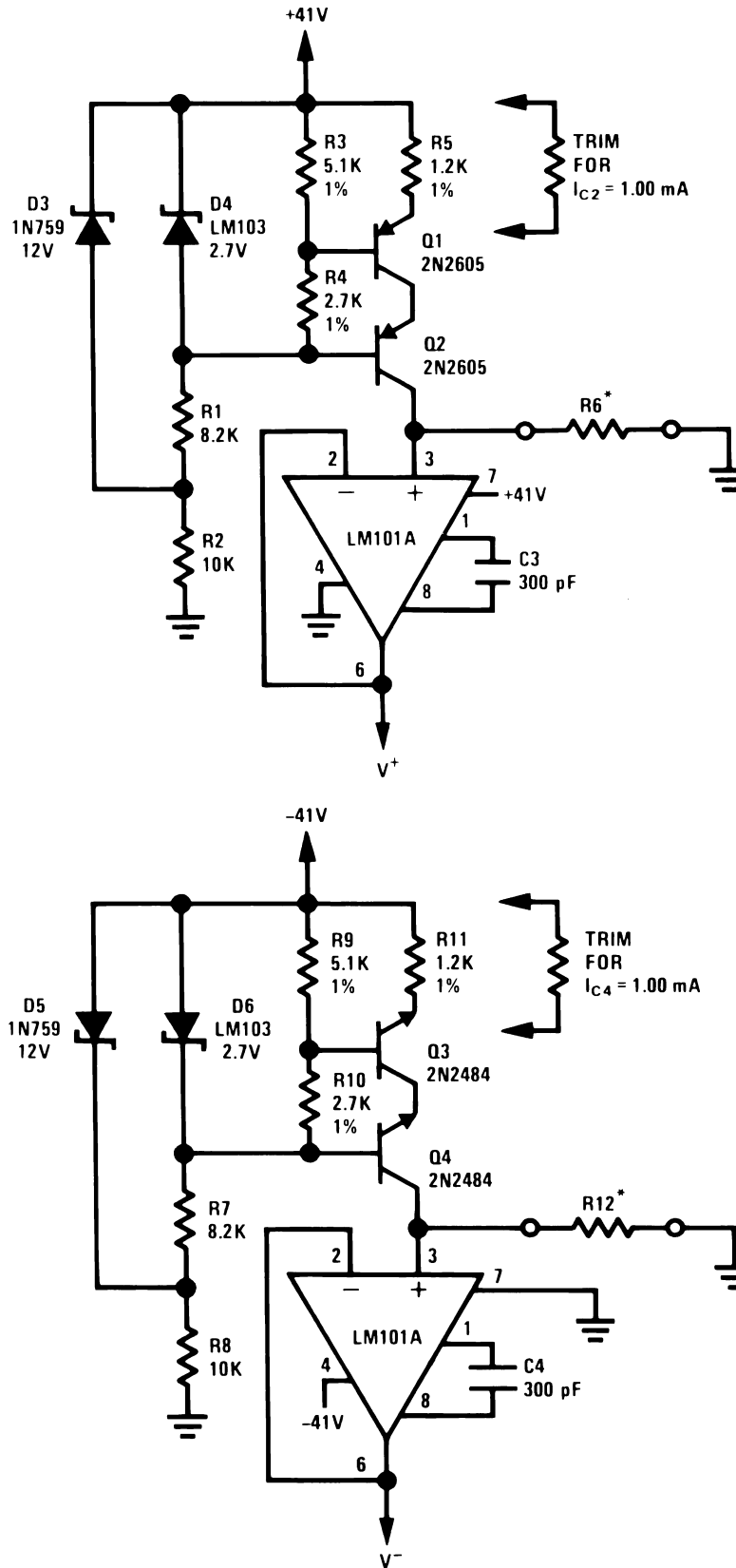


Figure 34. Wein Bridge Oscillator with FET Amplitude Stabilization



\* V<sub>OUT</sub> = 1V/kΩ

Figure 35. Low Power Supply for Integrated Circuit Testing

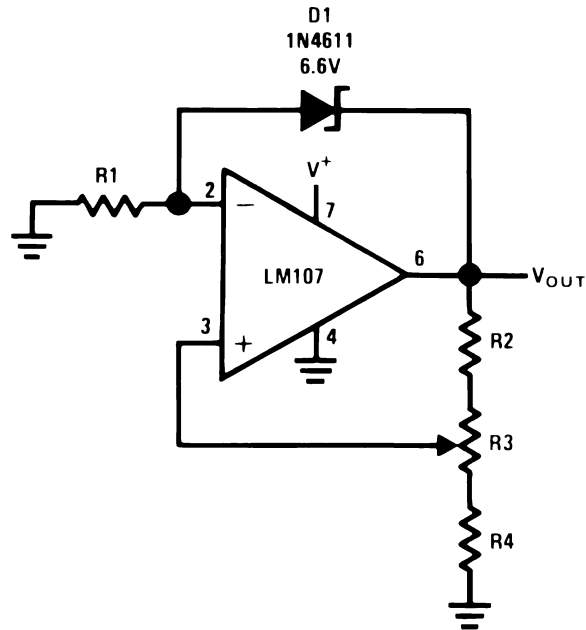


Figure 36. Positive Voltage Reference

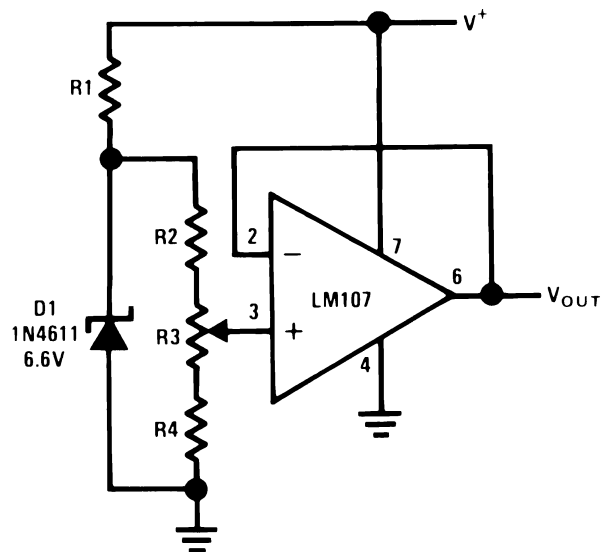


Figure 37. Positive Voltage Reference

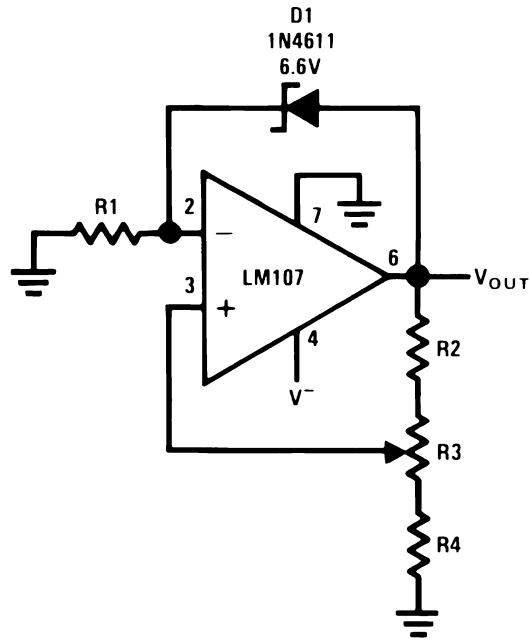


Figure 38. Negative Voltage Reference

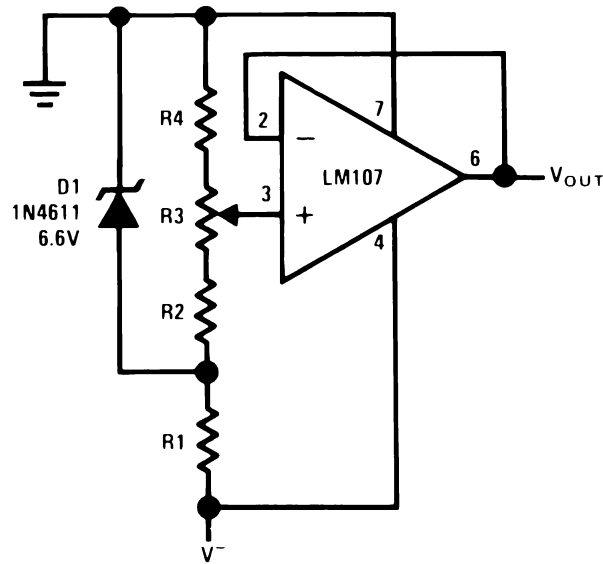


Figure 39. Negative Voltage Reference

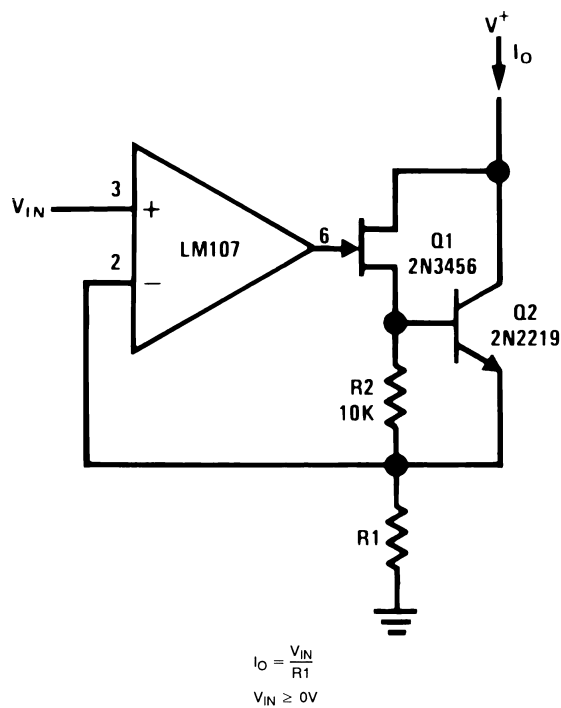


Figure 40. Precision Current Sink

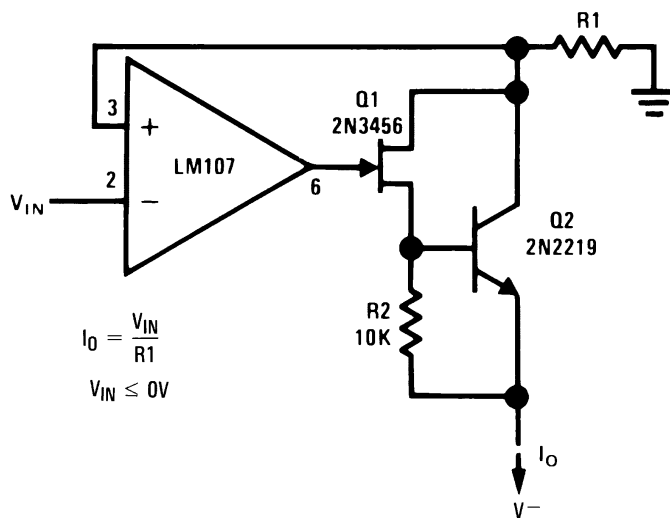


Figure 41. Precision Current Source



4 Signal Processing

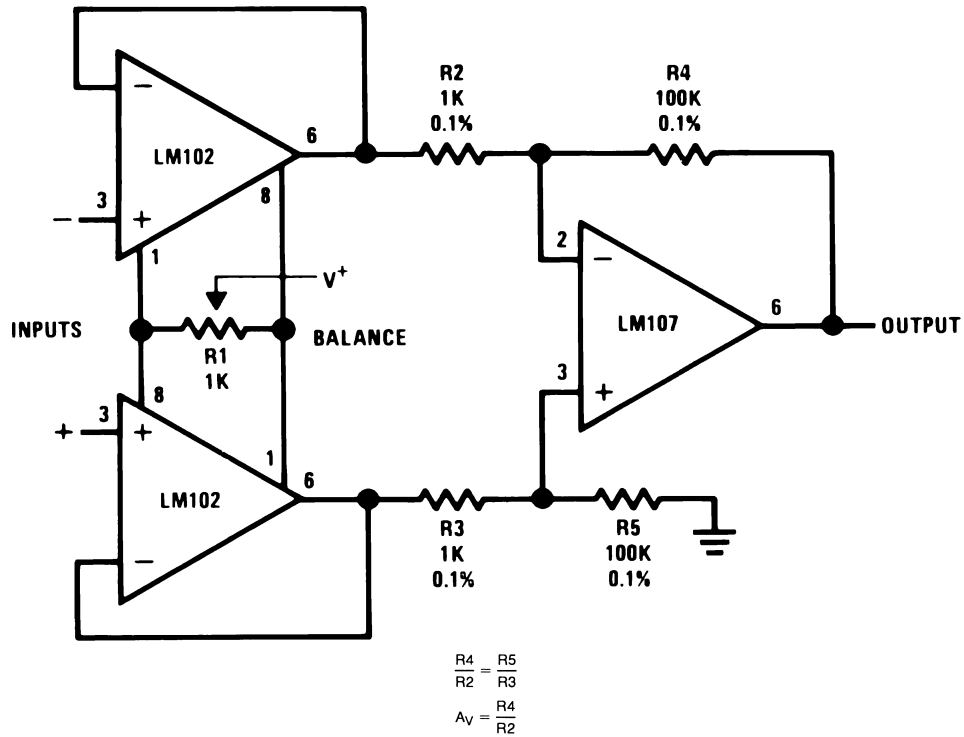
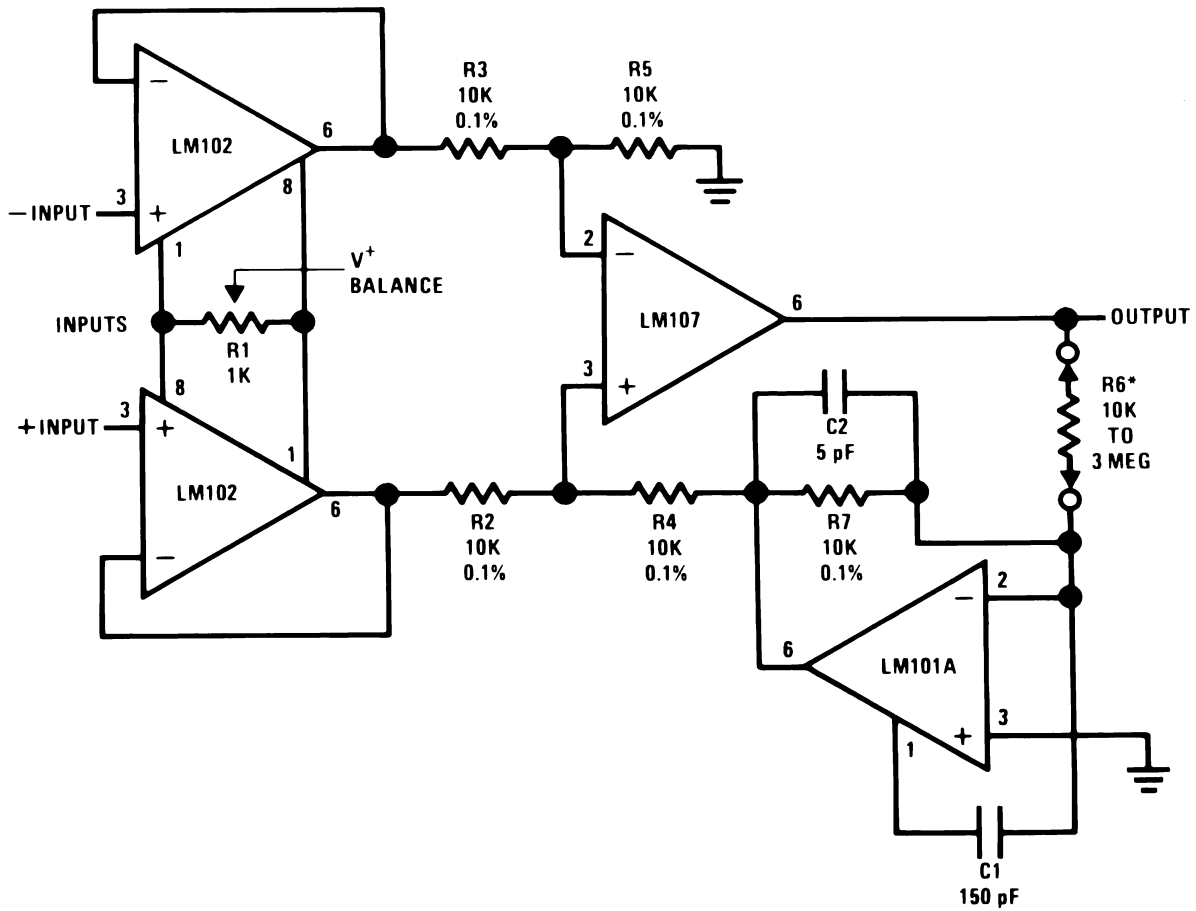
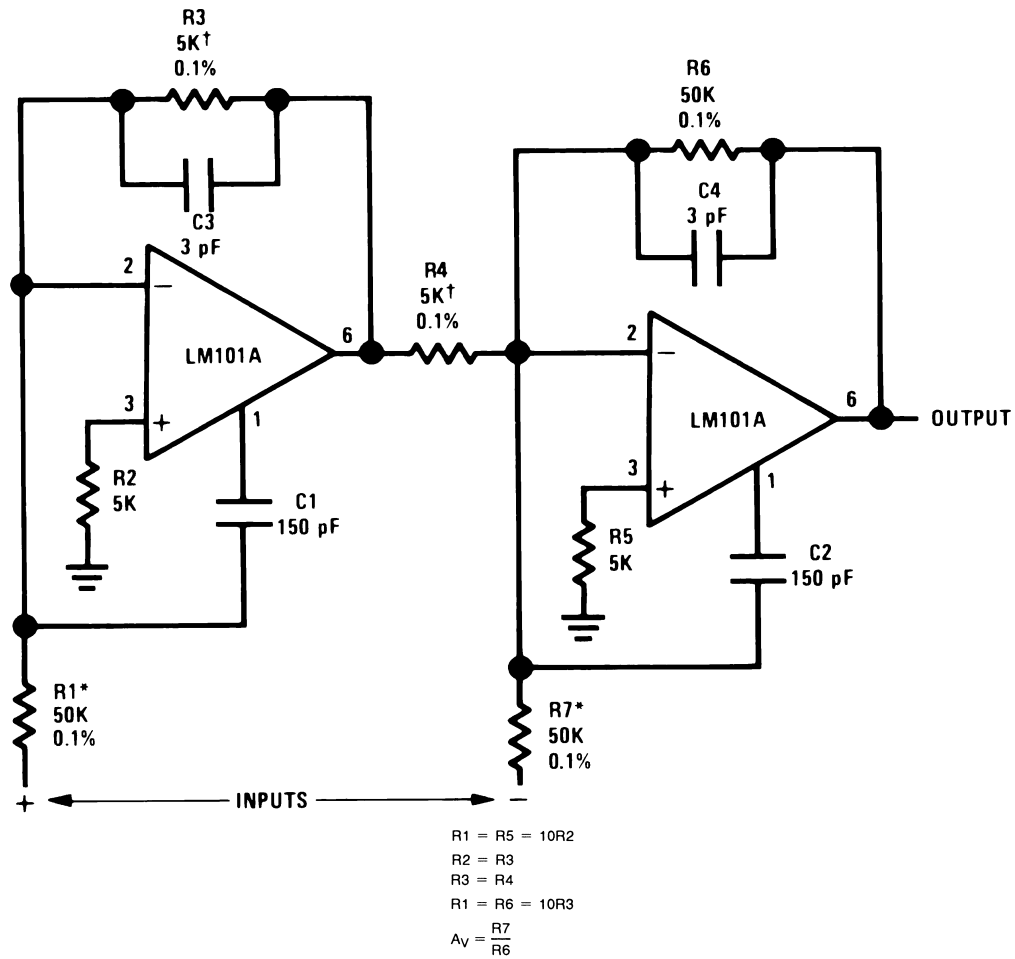


Figure 42. Differential-Input Instrumentation Amplifier



\* Gain adjust  $A_v = 10^{-4} R_6$

**Figure 43. Variable Gain, Differential-Input Instrumentation Amplifier**



† Matching determines common mode rejection.

**Figure 44. Instrumentation Amplifier with ±100 Volt Common Mode Range**

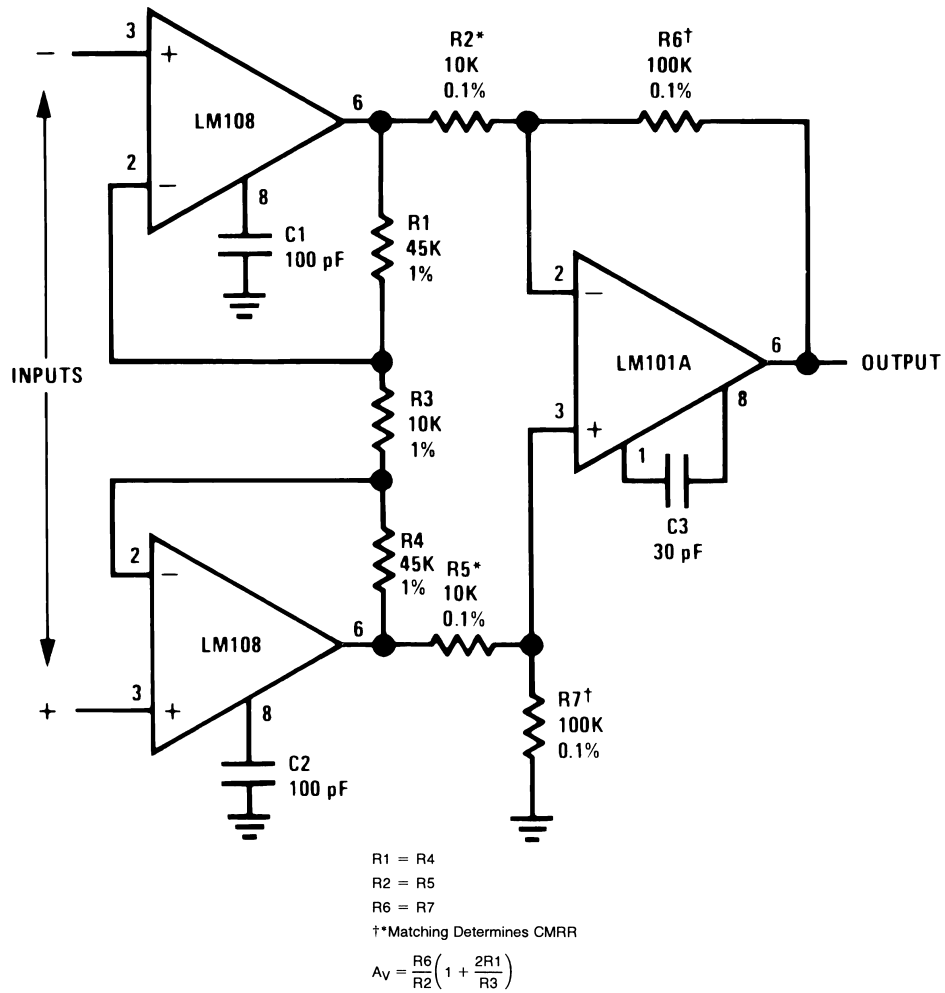
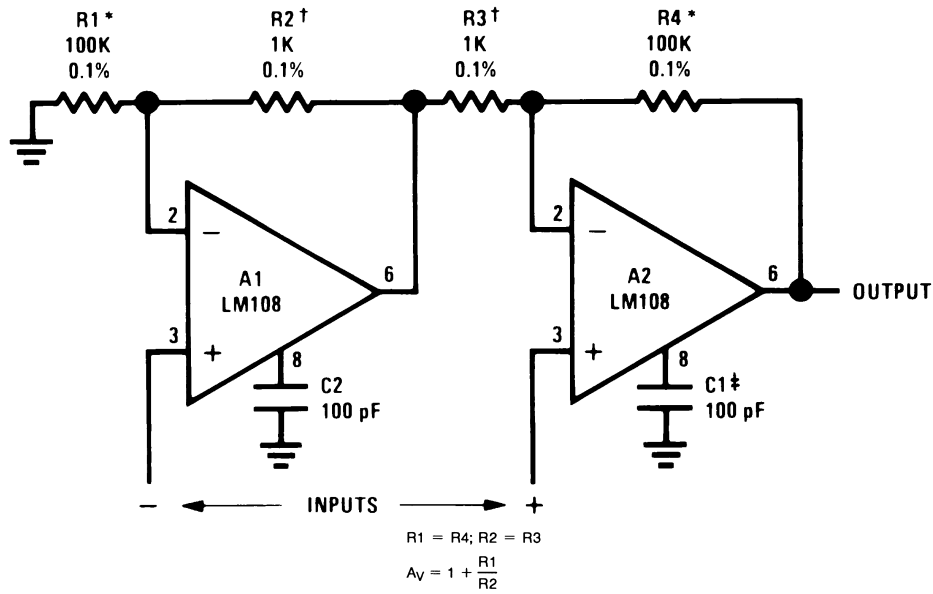
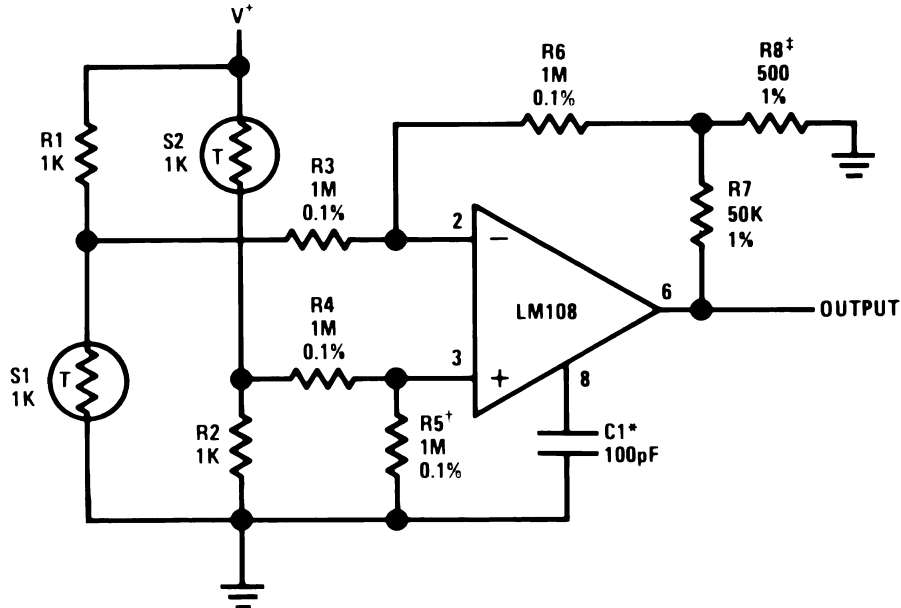


Figure 45. Instrumentation Amplifier with ±10 Volt Common Mode Range



\*† Matching Determines CMRR  
 ‡ May be deleted to maximize bandwidth

Figure 46. High Input Impedance Instrumentation Amplifier



\* Reduces feed through of power supply noise by 20 dB and makes supply bypassing unnecessary.  
 † Trim for best common mode rejection  
 ‡ Gain adjust

Figure 47. Bridge Amplifier with Low Noise Compensation

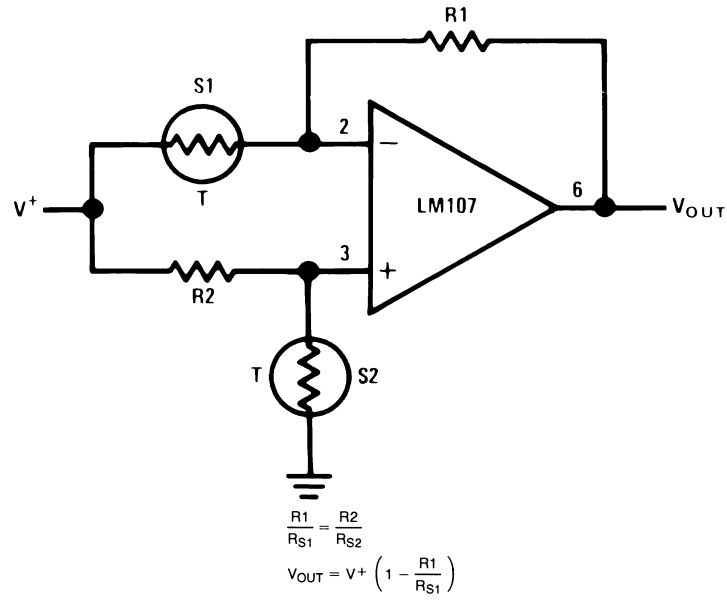


Figure 48. Bridge Amplifier

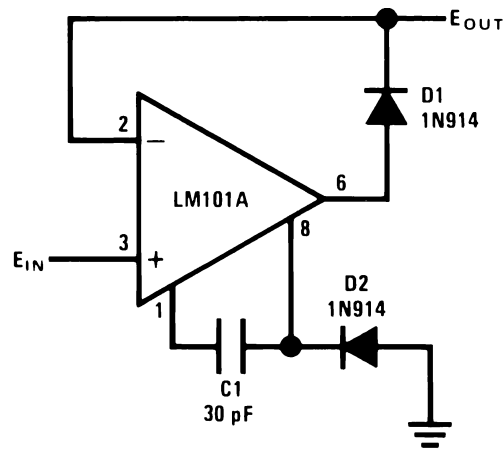
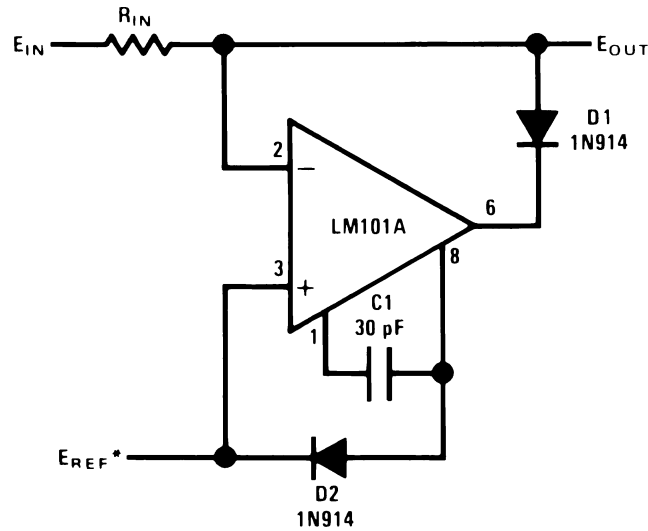


Figure 49. Precision Diode



\*  $E_{REF}$  must have a source impedance of less than  $200\Omega$  if D2 is used.

Figure 50. Precision Clamp

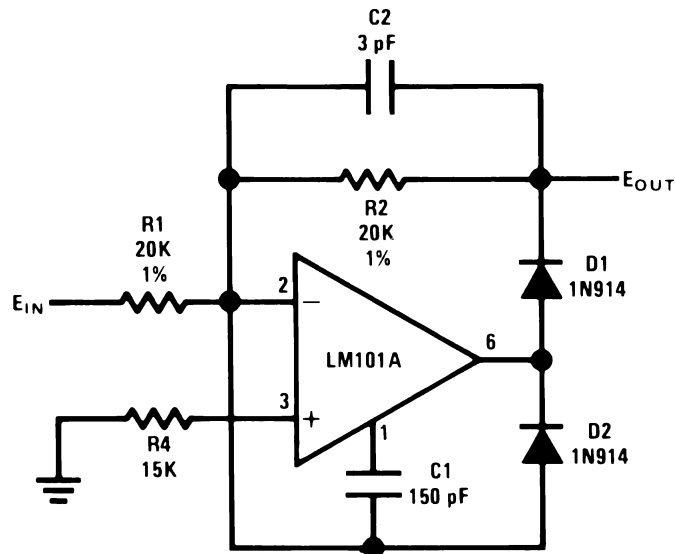
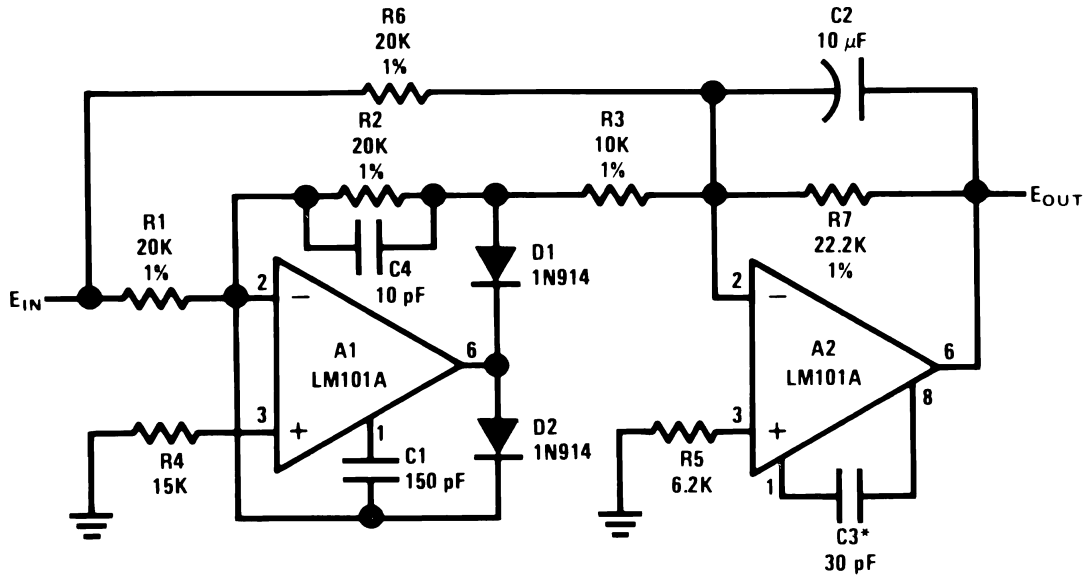


Figure 51. Fast Half Wave Rectifier



\* Feedforward compensation can be used to make a fast full wave rectifier without a filter.

Figure 52. Precision AC to DC Converter

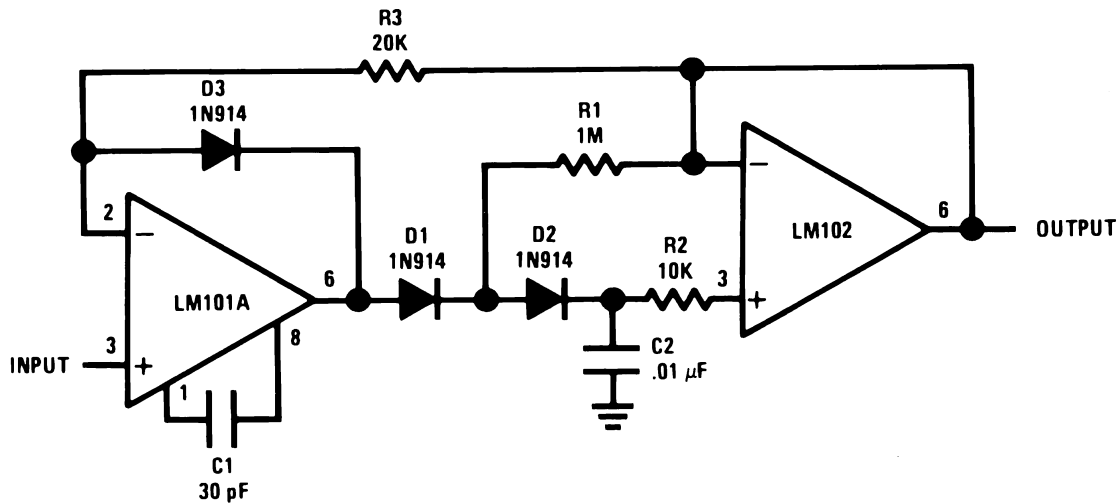


Figure 53. Low Drift Peak Detector



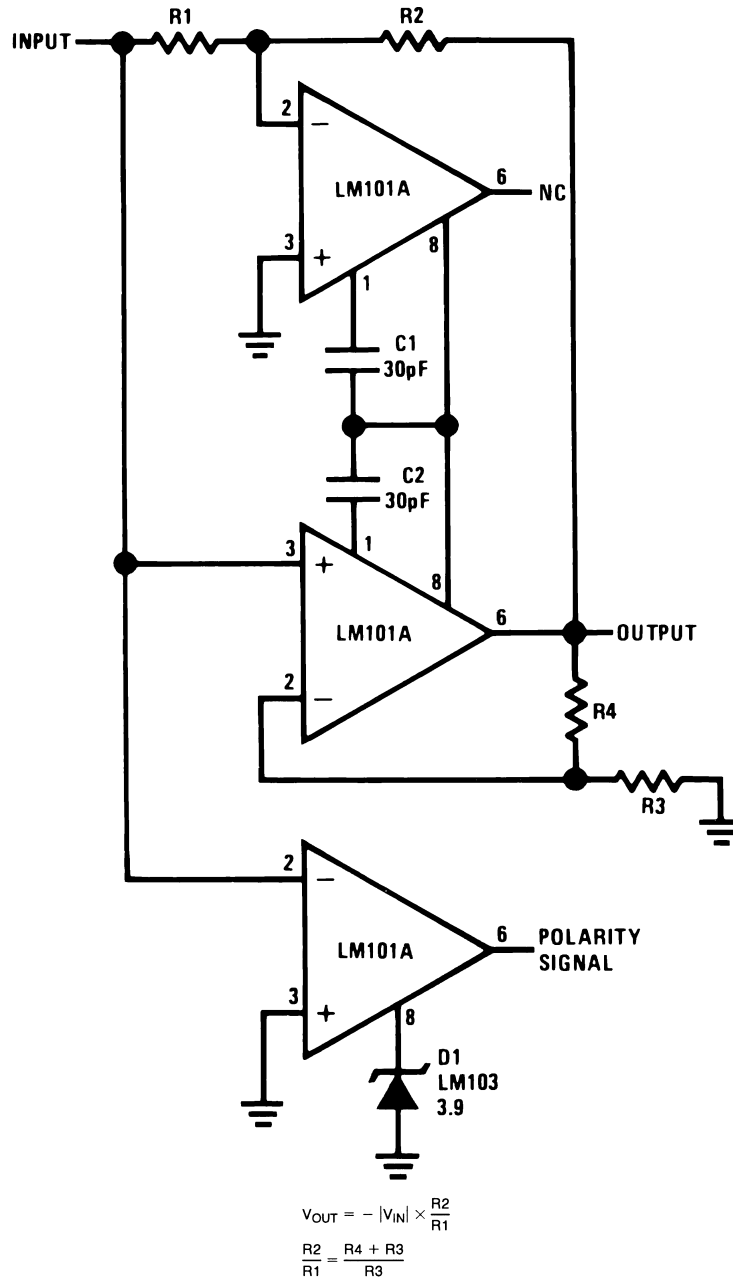
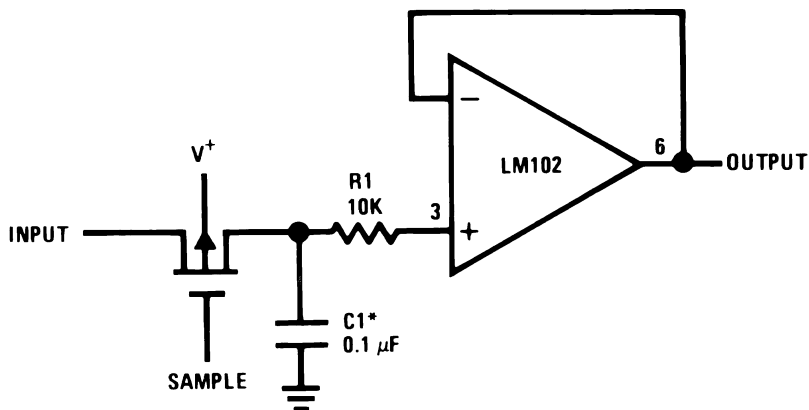
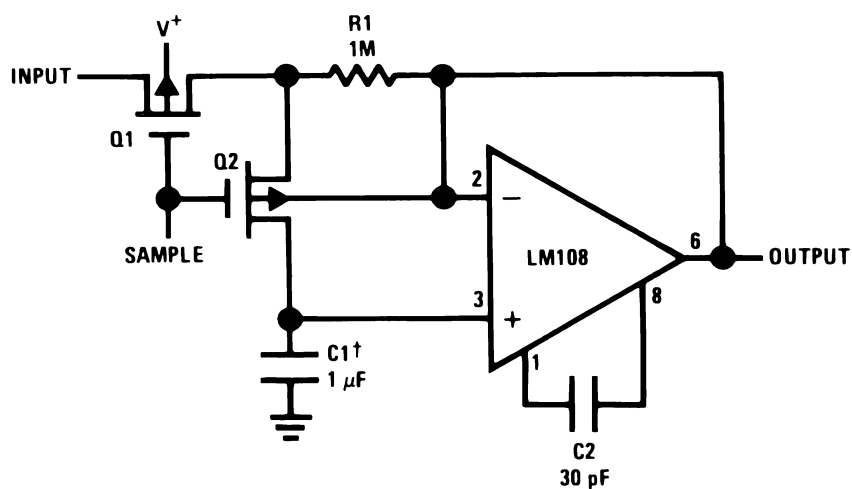


Figure 54. Absolute Value Amplifier with Polarity Detector



\* Polycarbonate-dielectric capacitor

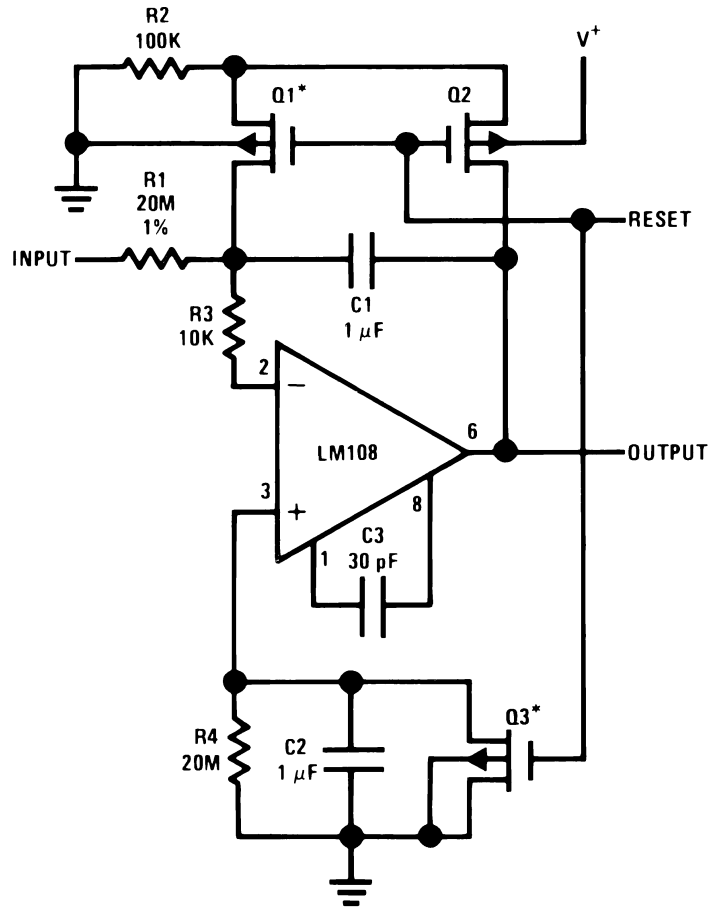
Figure 55. Sample and Hold



\* Worst case drift less than 2.5 mV/sec

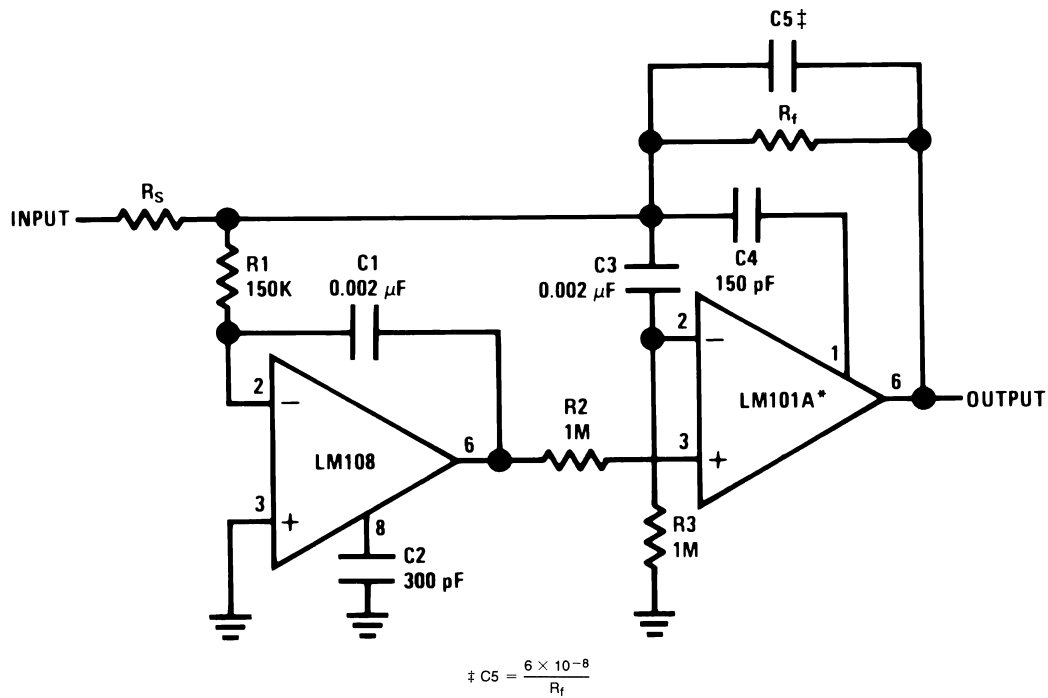
† Teflon, Polyethylene or Polycarbonate Dielectric Capacitor

Figure 56. Sample and Hold



\* Q1 and Q3 should not have internal gate-protection diodes.  
 Worst case drift less than 500 μV/sec over -55°C to +125°C.

**Figure 57. Low Drift Integrator**



\* In addition to increasing speed, the LM101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

† Power Bandwidth: 250 kHz

Small Signal Bandwidth: 3.5 MHz

Slew Rate: 10V/μs

**Figure 58. Fast<sup>†</sup> Summing Amplifier with Low Input Current**

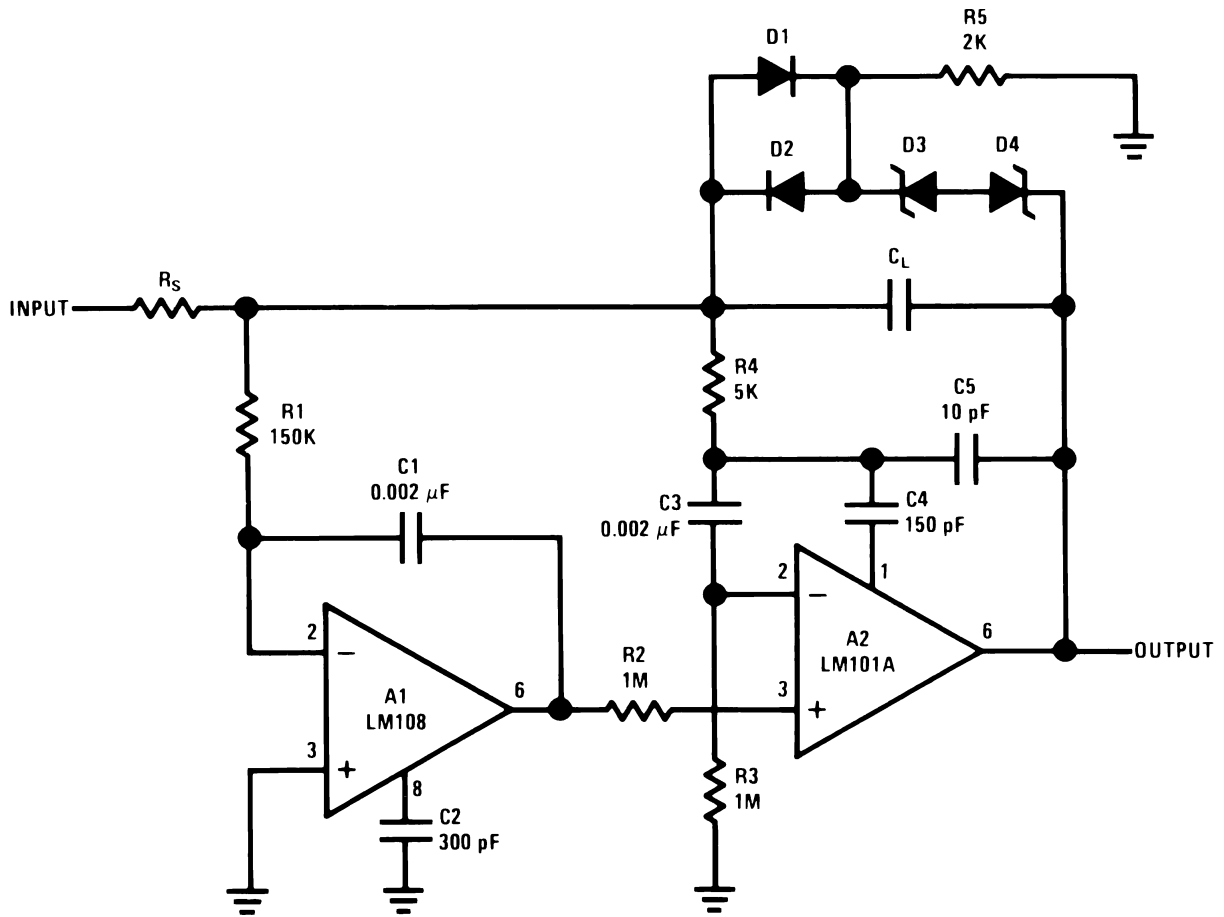
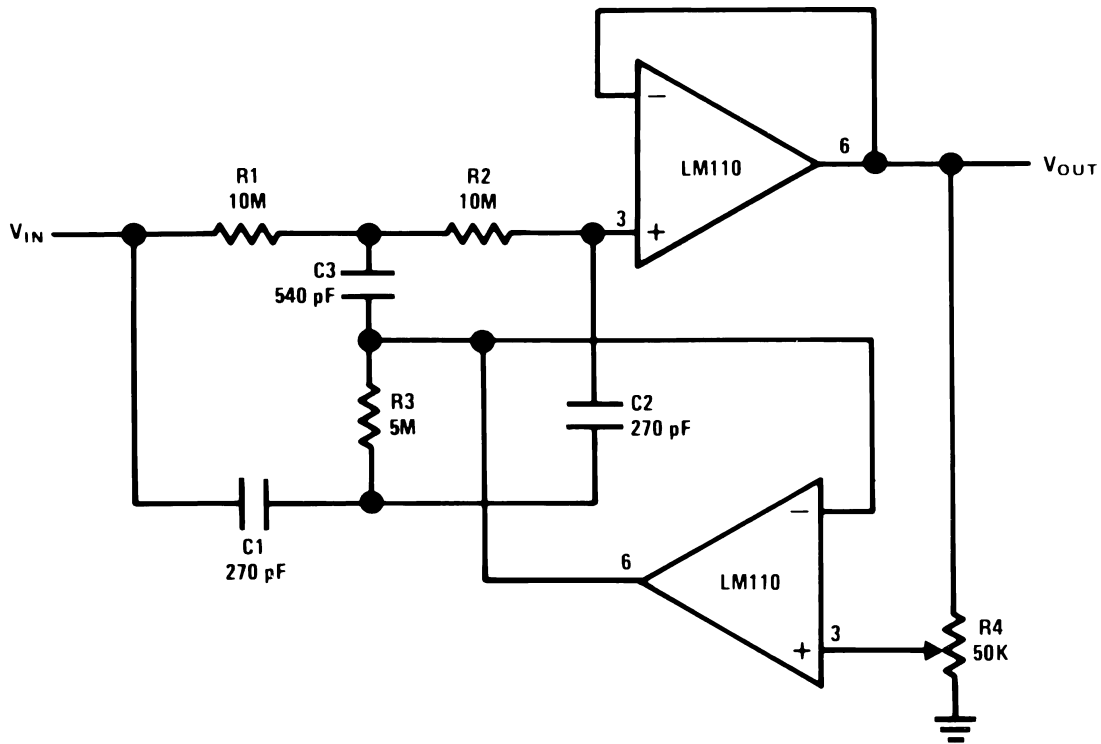


Figure 59. Fast Integrator with Low Input Current



$$f_o = \frac{1}{2\pi R_1 C_1}$$

$$= 60 \text{ Hz}$$

$$R_1 = R_2 = R_3$$

$$C_1 = C_2 = C_3$$

Figure 60. Adjustable Q Notch Filter

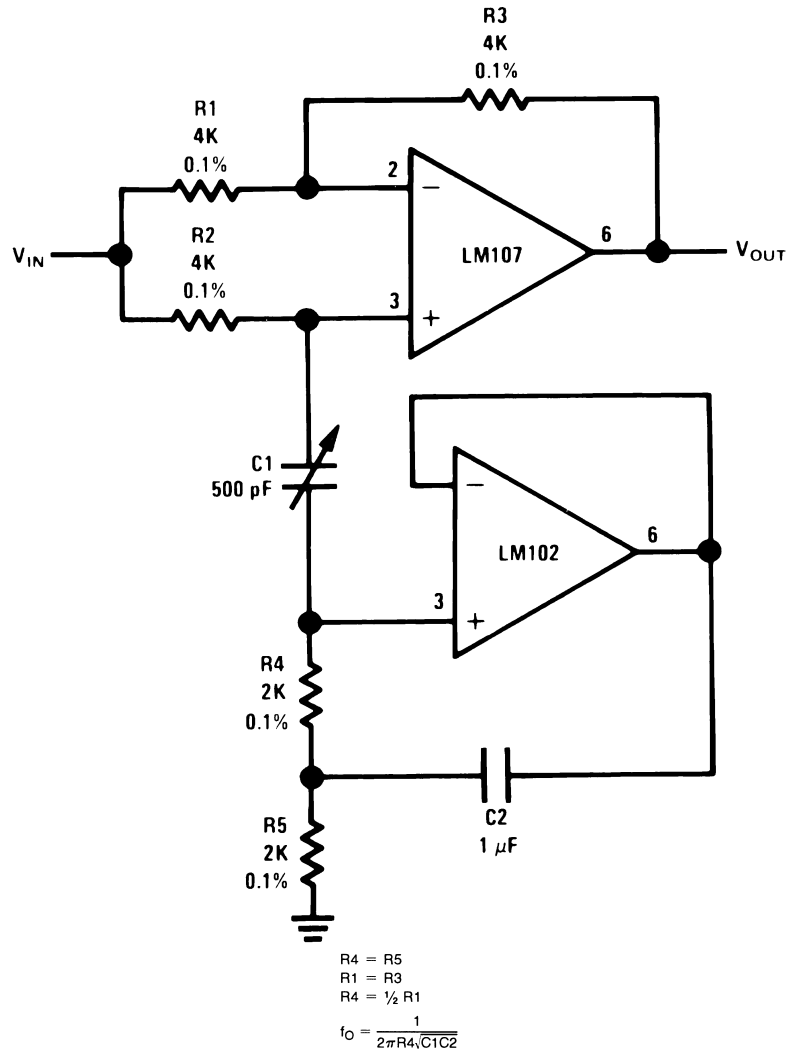


Figure 61. Easily Tuned Notch Filter

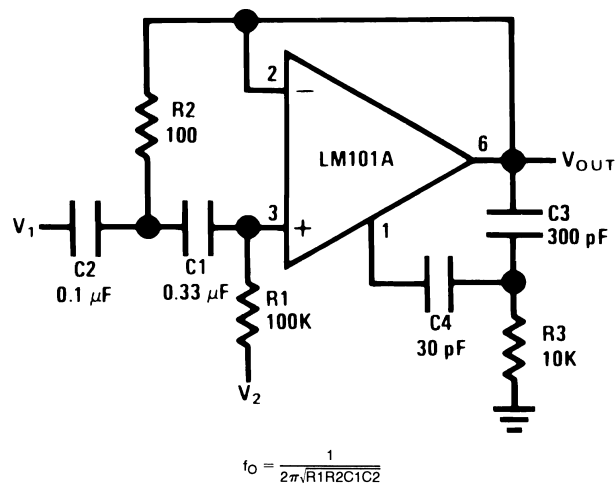


Figure 62. Tuned Circuit

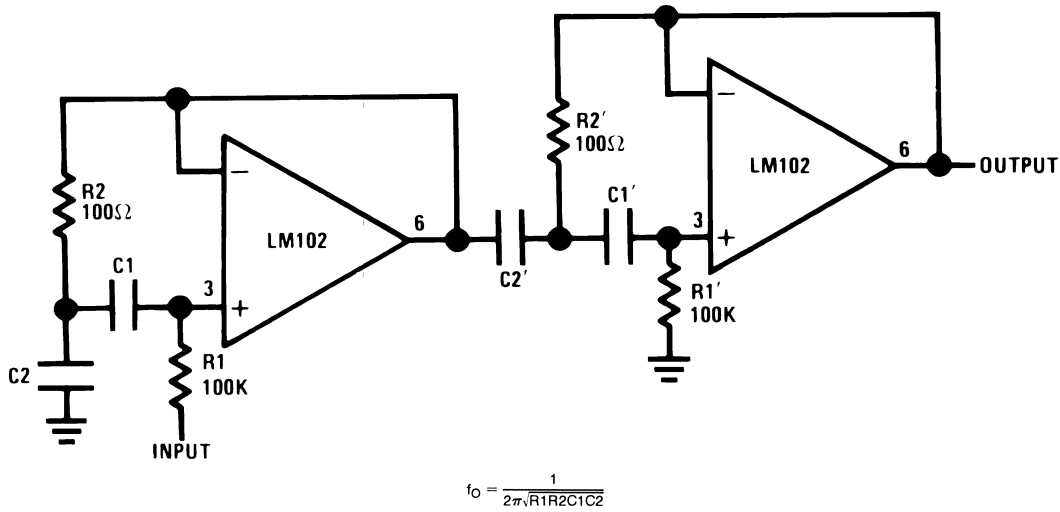


Figure 63. Two-Stage Tuned Circuit

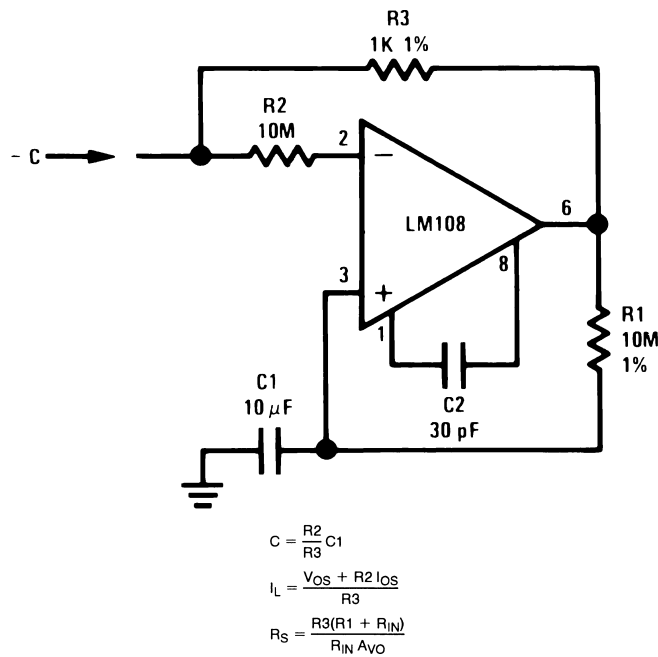


Figure 64. Negative Capacitance Multiplier



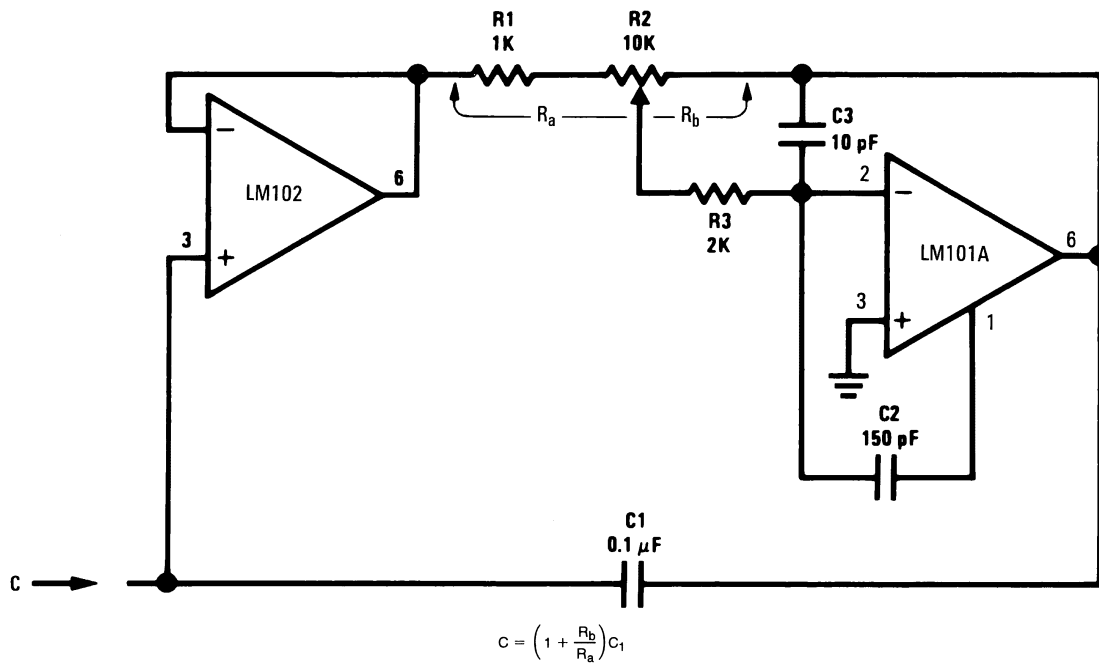
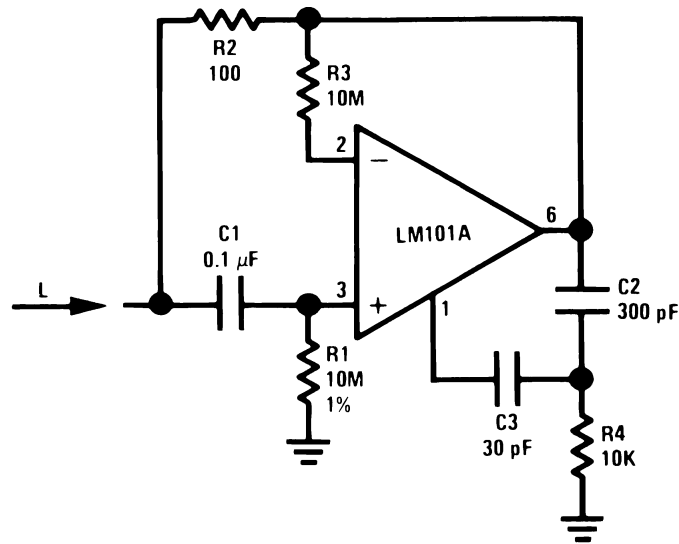


Figure 65. Variable Capacitance Multiplier



$$L \geq R_1 R_2 C_1$$

$$R_s = R_2$$

$$R_p = R_1$$

Figure 66. Simulated Inductor

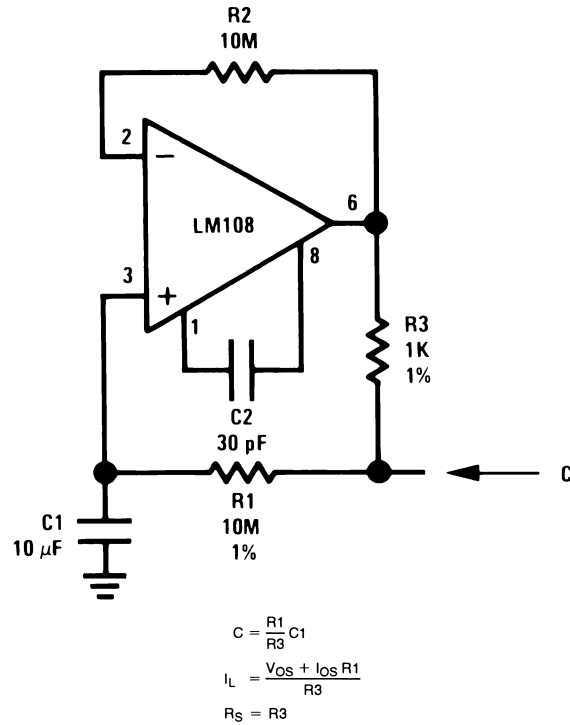
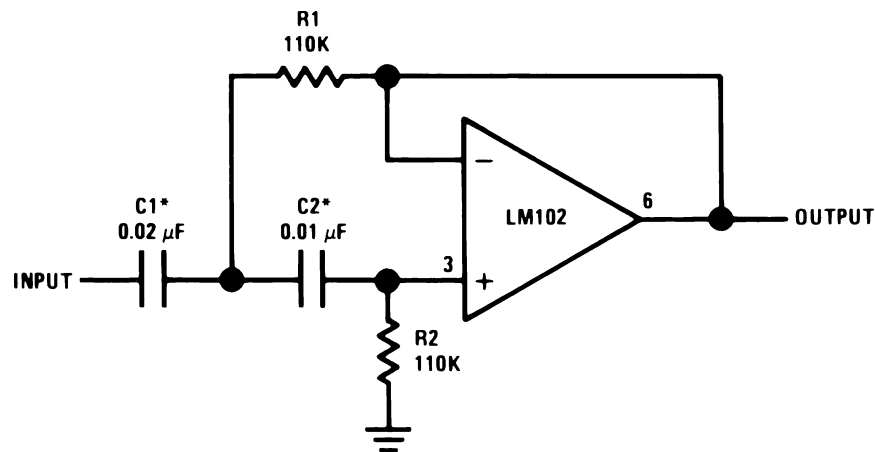
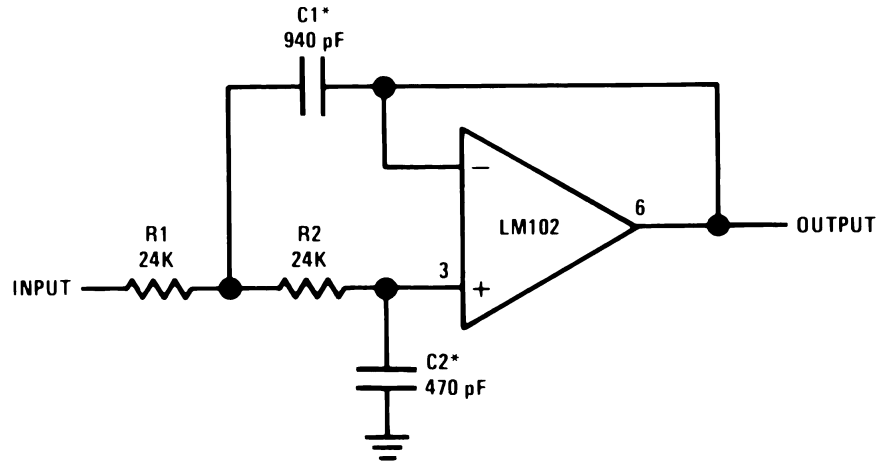


Figure 67. Capacitance Multiplier



\* Values are for 100 Hz cutoff. Use metallized polycarbonate capacitors for good temperature stability.

Figure 68. High Pass Active Filter



\* Values are for 10 kHz cutoff. Use silvered mica capacitors for good temperature stability.

Figure 69. Low Pass Active Filter

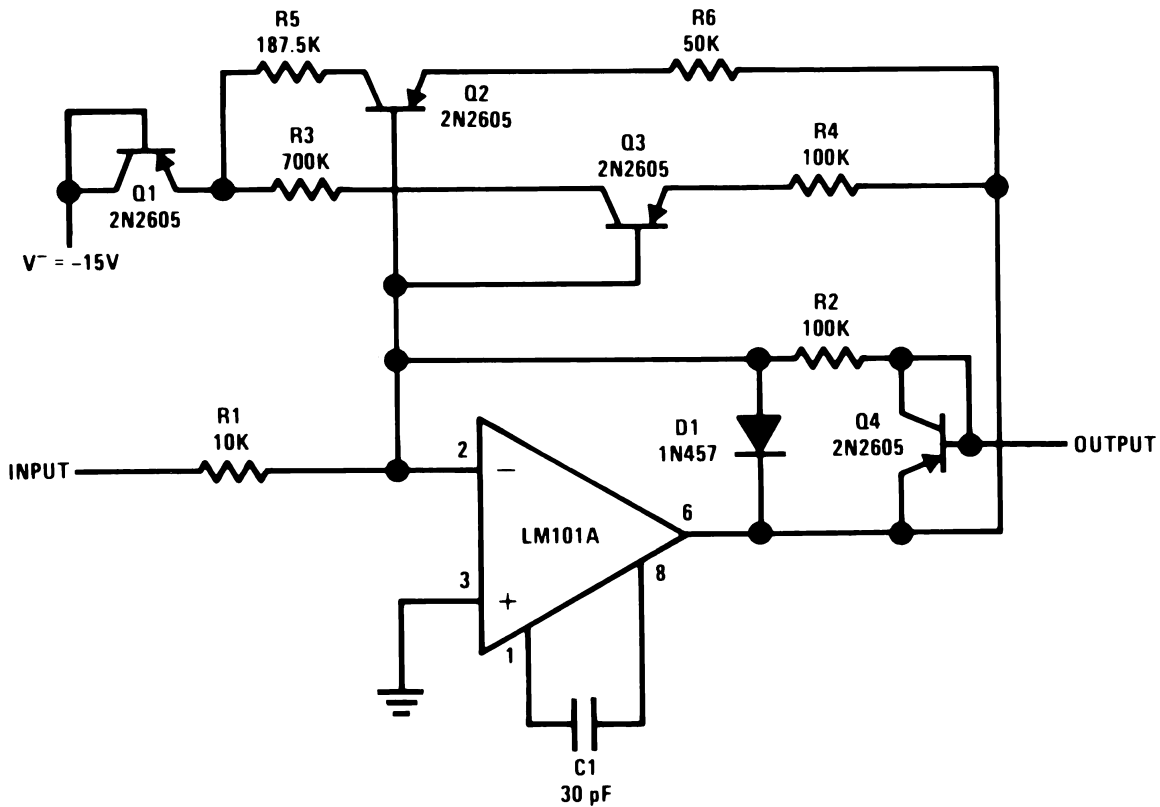


Figure 70. Nonlinear Operational Amplifier with Temperature Compensated Breakpoints

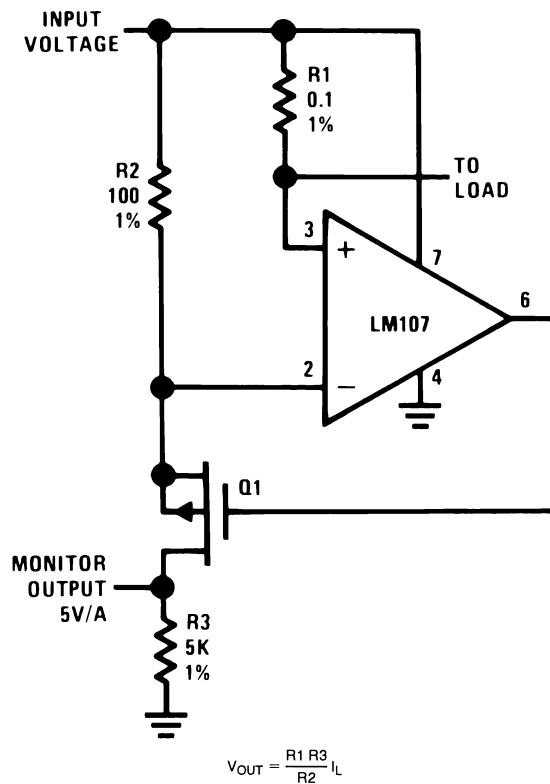


Figure 71. Current Monitor

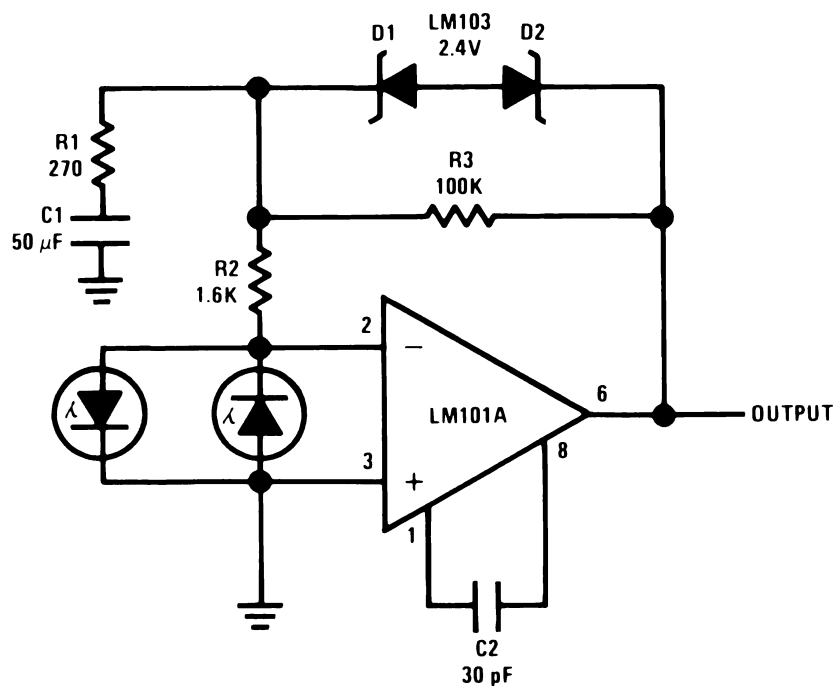


Figure 72. Saturating Servo Preamplifier with Rate Feedback

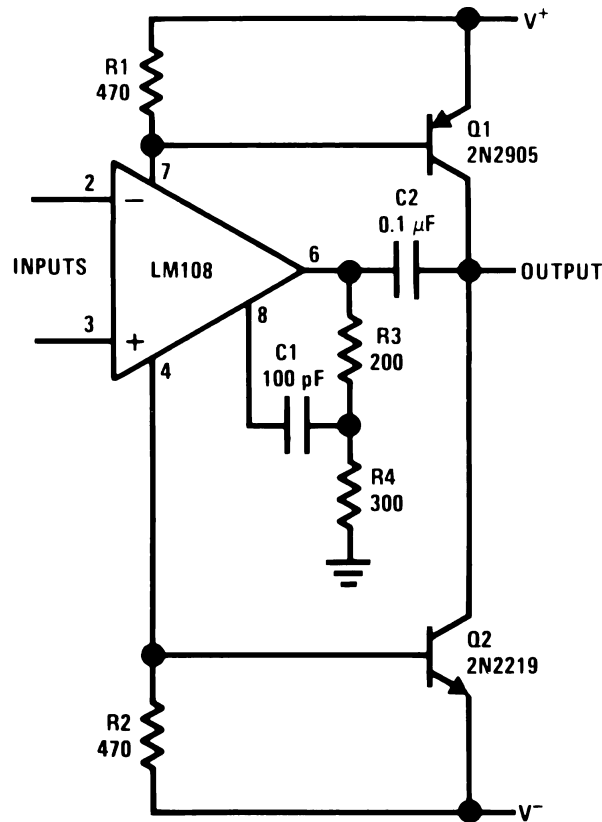


Figure 73. Power Booster

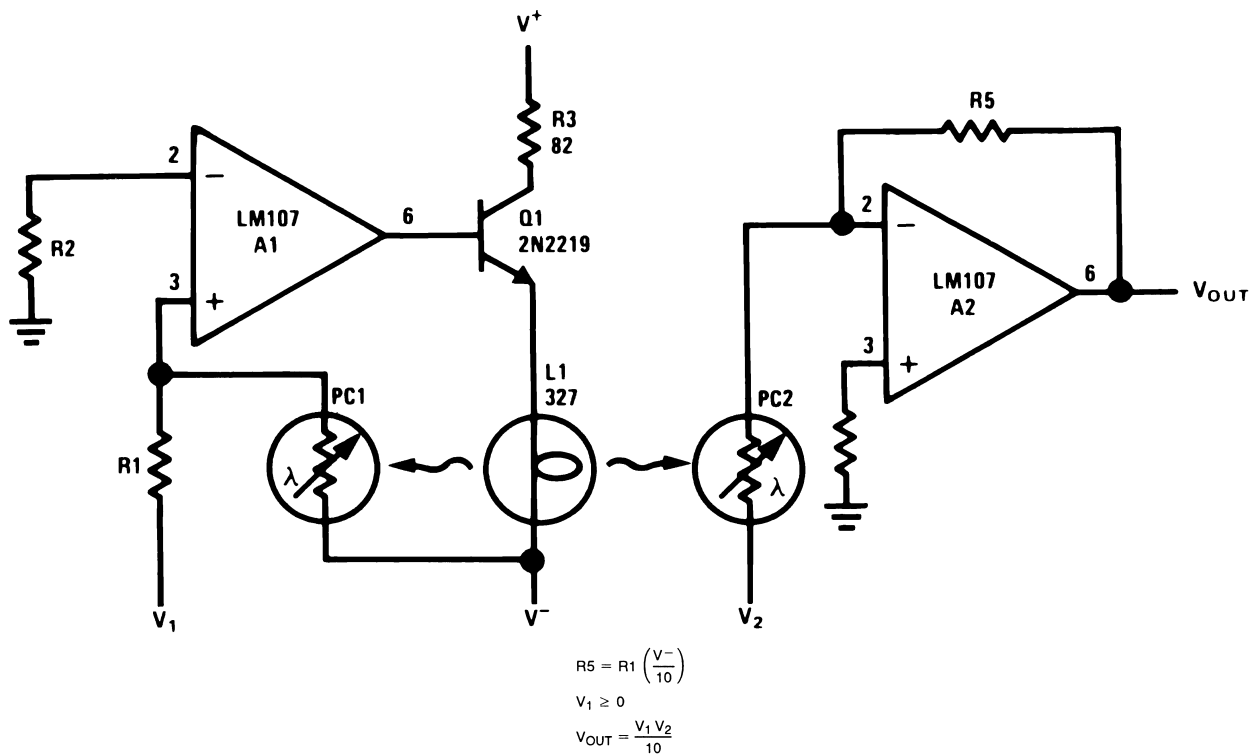
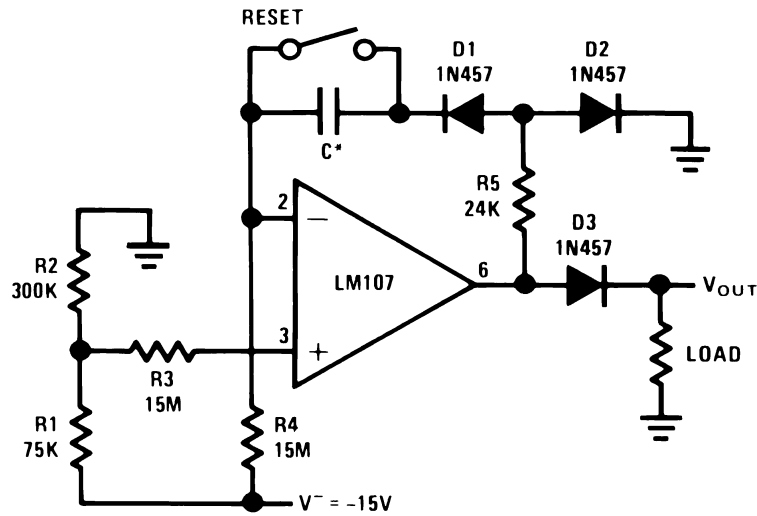
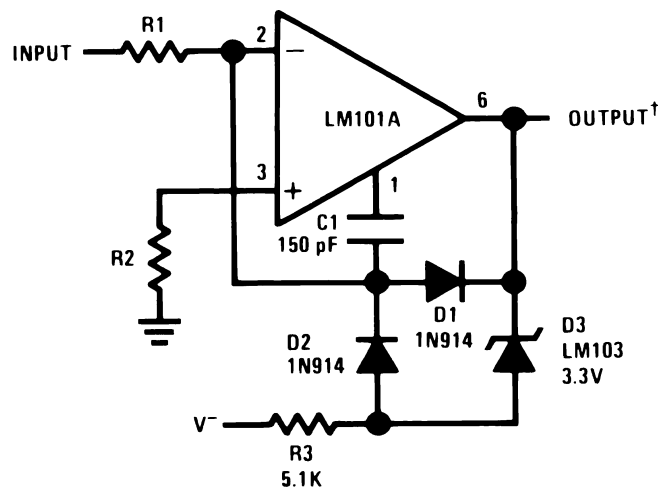


Figure 74. Analog Multiplier



\* Low leakage  $-0.017 \mu\text{F}$  per second delay

Figure 75. Long Interval Timer



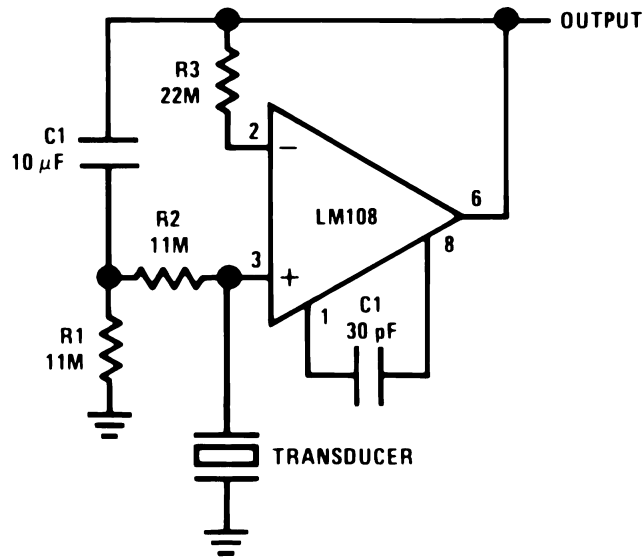
Propagation delay approximately 200 ns

† DTL or TTL fanout of three.

Minimize stray capacitance

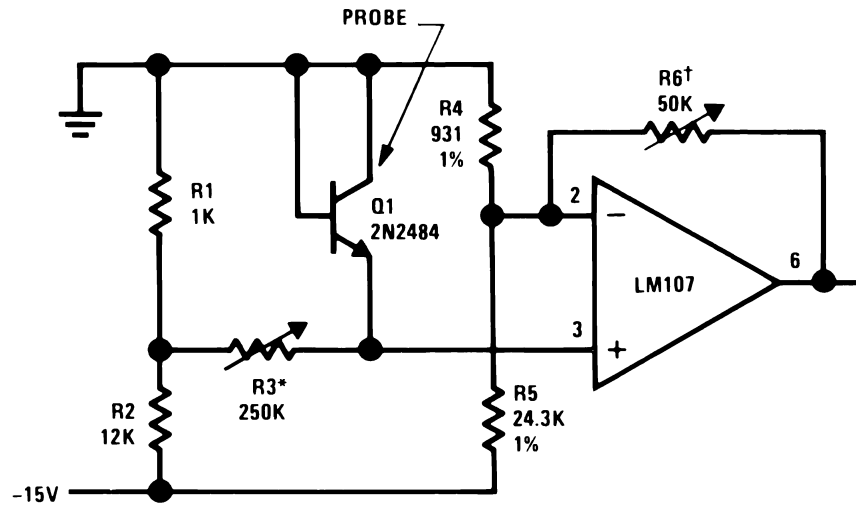
Pin 8

Figure 76. Fast Zero Crossing Detector



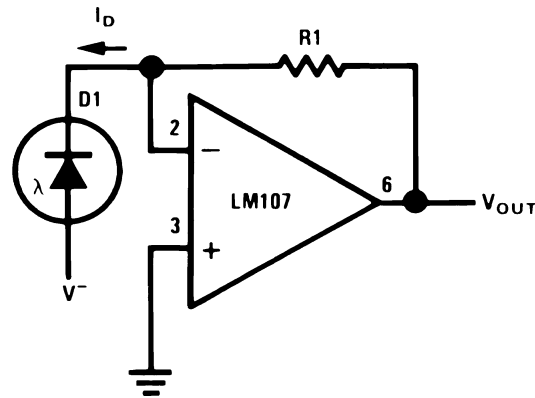
Low frequency cutoff =  $R1 C1$

Figure 77. Amplifier for Piezoelectric Transducer



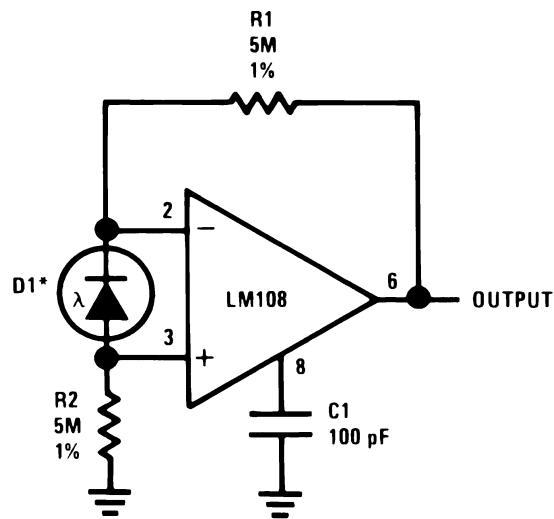
\* Set for 0V at 0°C  
 † Adjust for 100 mV/°C

Figure 78. Temperature Probe



$$V_{OUT} = R1 I_D$$

Figure 79. Photodiode Amplifier



$$V_{OUT} = 10 V/\mu A$$

\*Operating photodiode with less than 3 mV across it eliminates leakage currents.

Figure 80. Photodiode Amplifier

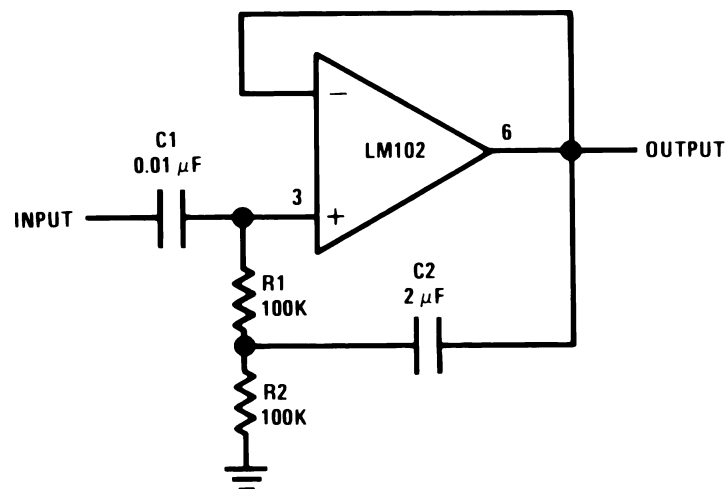
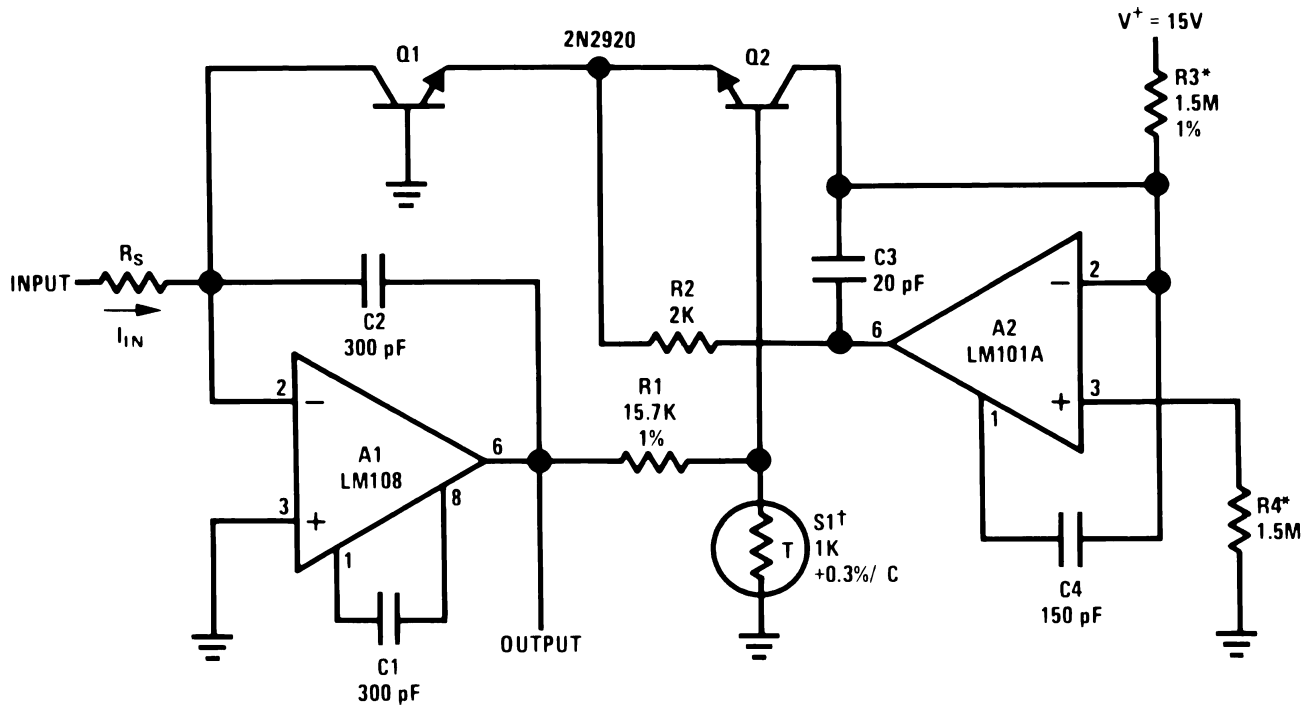


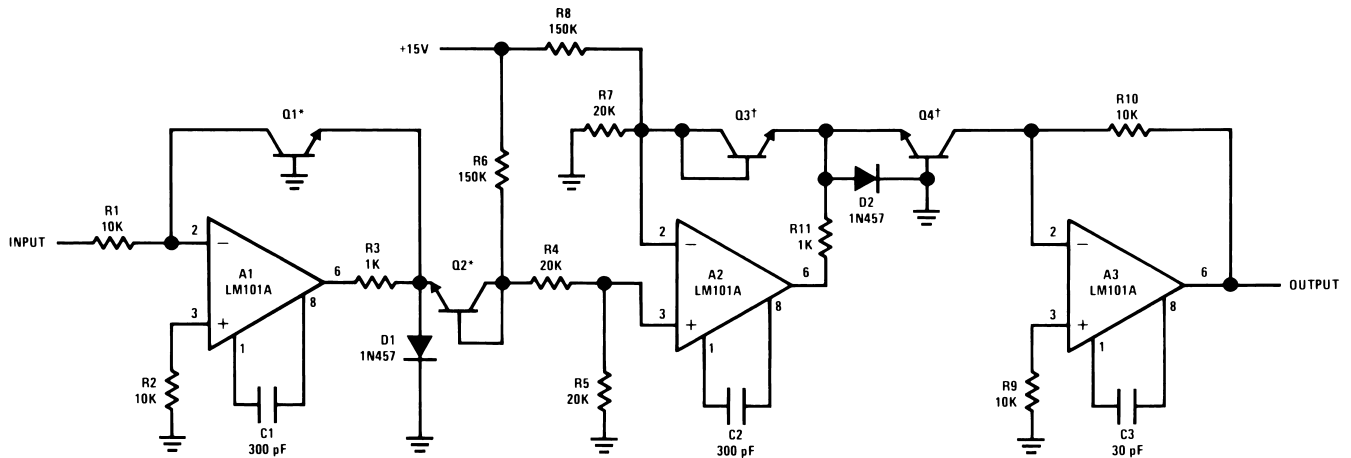
Figure 81. High Input Impedance AC Follower





10 nA <  $I_{IN}$  < 1 mA  
 Sensitivity is 1V per decade  
 † 1 k $\Omega$  ( $\pm 1\%$ ) at 25°C, +3500 ppm/°C.  
 Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.  
 \* Determines current for zero crossing on output: 10  $\mu$ A as shown.

Figure 82. Temperature Compensated Logarithmic Converter



\*† 2N3728 matched pairs

Figure 83. Root Extractor

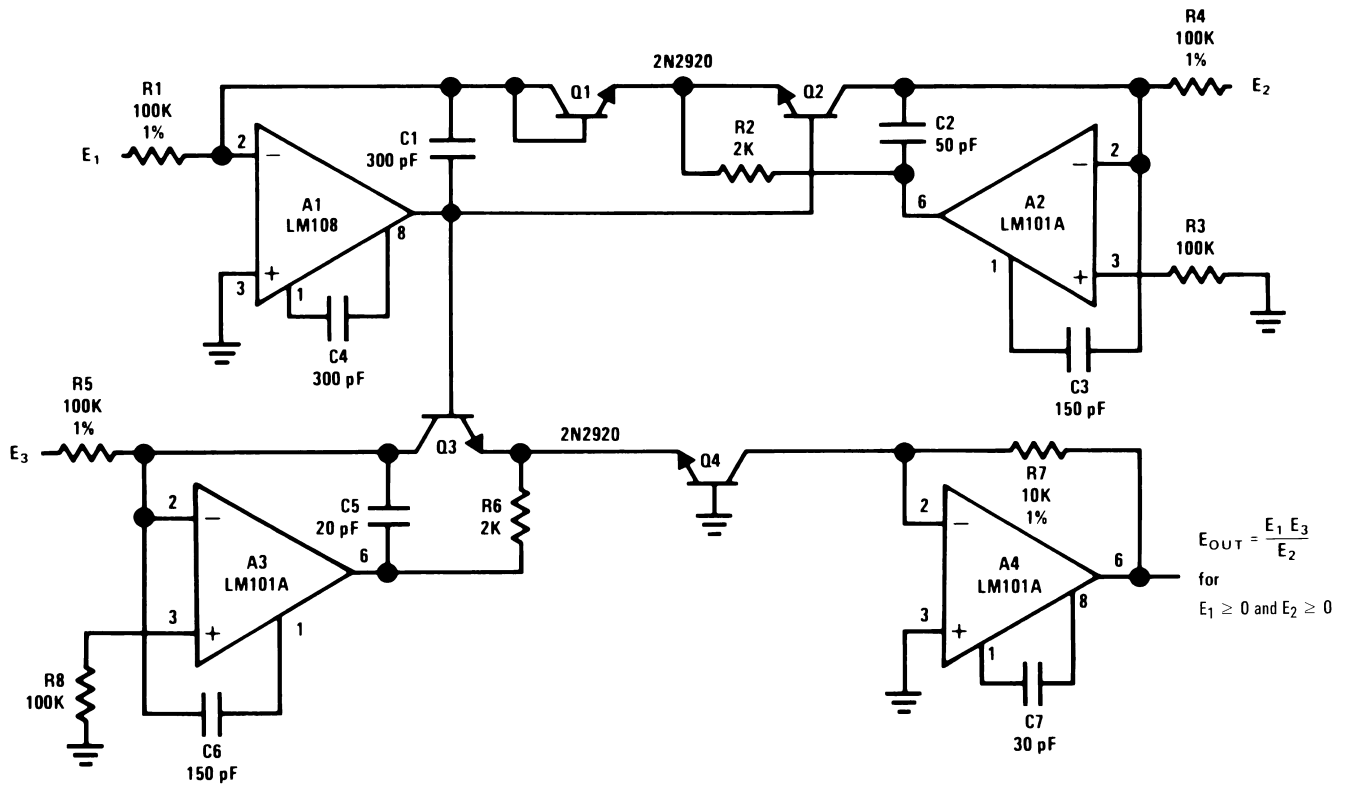


Figure 84. Multiplier/Divider

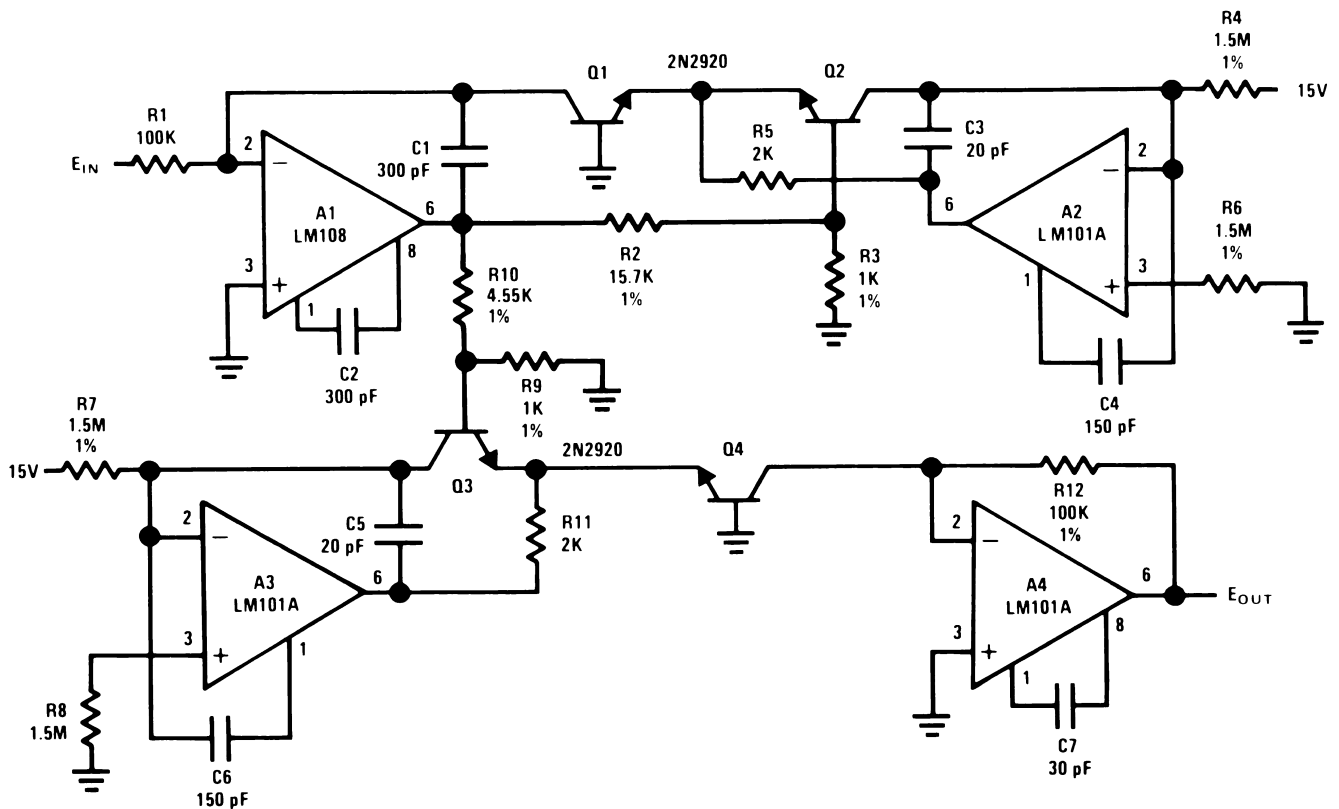
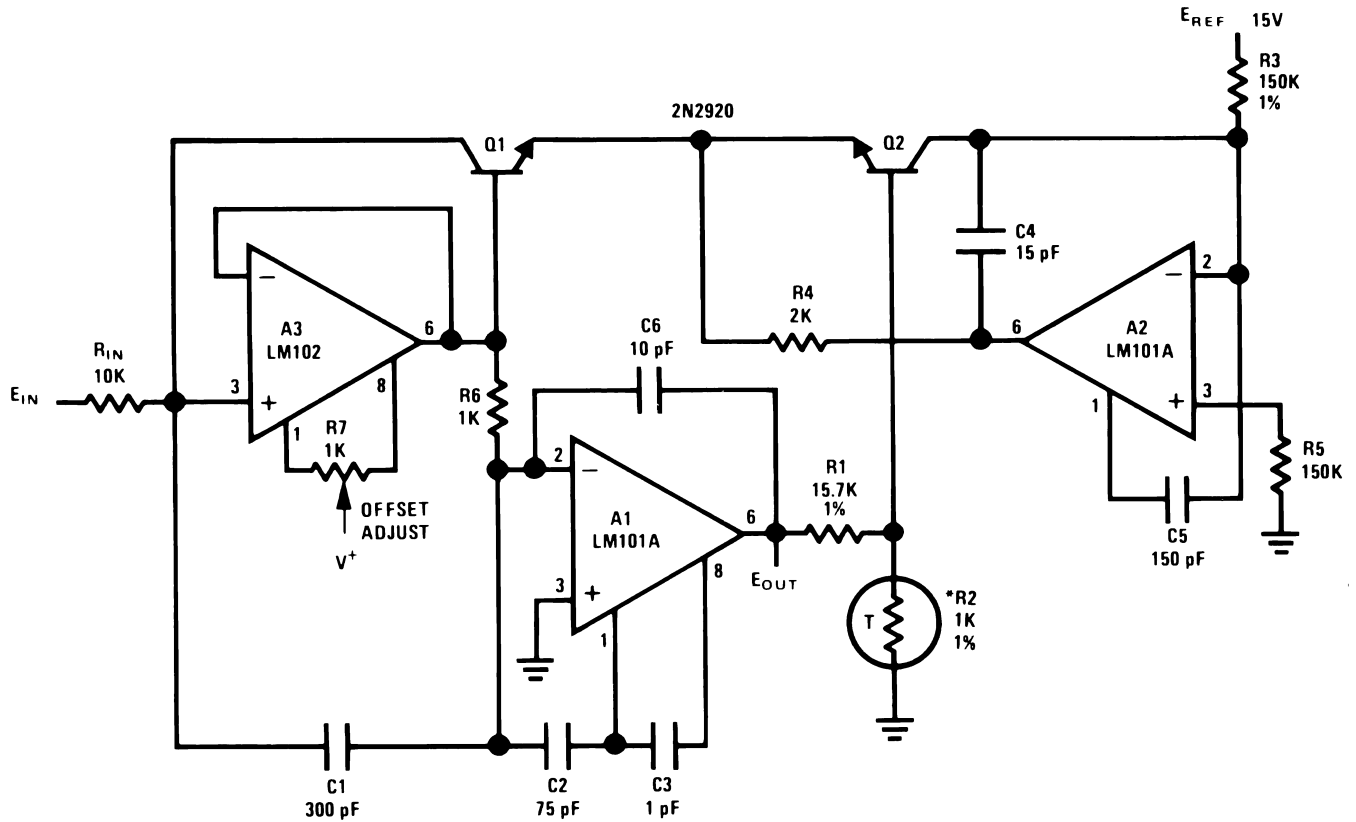
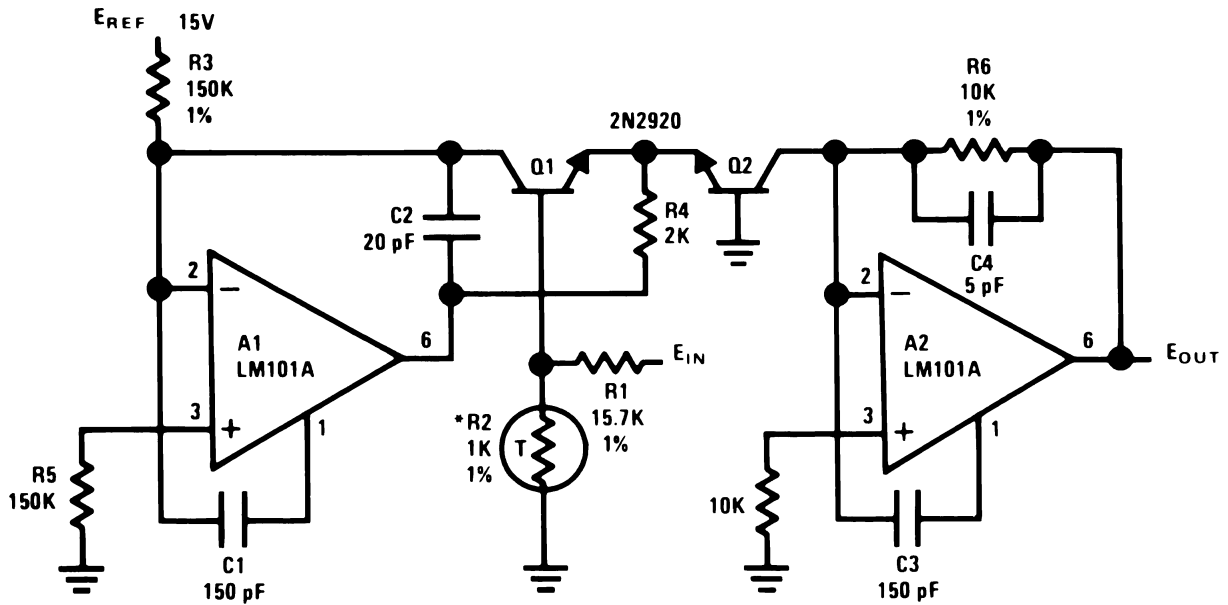


Figure 85. Cube Generator



† 1 k $\Omega$  ( $\pm 1\%$ ) at 25°C, +3500 ppm/°C.  
 Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

Figure 86. Fast Log Generator



† 1 k $\Omega$  ( $\pm 1\%$ ) at 25°C, +3500 ppm/°C.  
 Available from Vishay Ultronix, Grand Junction, CO, Q81 Series.

Figure 87. Anti-Log Generator

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