M-991 Call Progress Tone Generator

- **Generates standard call progress tones**
- **Digital input control**
- **Linear (analog) output**
- **Power output capable of driving standard line**
- **14-pin DIP and 16-pin SOIC package types**
- **Single supply 5V CMOS (low power)**
- **Inexpensive 3.58 MHz time base**
- **Temperature range from -25° to 70° (-01 version)**
- **Temperature range from -40° to 85° (-02 version)**
- **Applications include: telephone systems, test equipment, callback security systems, billing systems, audible alert systems**

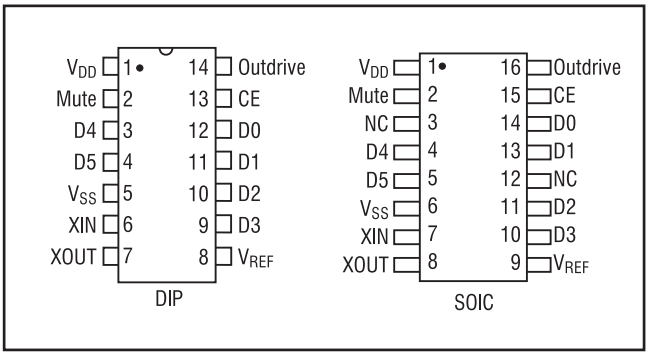


Figure 1 Pin Diagrams

The Teltone M-991 is a call progress tone generator integrated circuit for use in telephone systems. The circuit uses low-power CMOS techniques to generate tones which are digitally controlled and highly linear. The M-991 is designed to permit operation with almost any system. The use of integrated circuit techniques allows the M-991 to incorporate the control, tone generating, and power output buffer into a single 14-pin DIP or a 16-pin SOIC. A 3.58-MHz (color burst) crystal-controlled time base guarantees accuracy and repeatability.

Call Progress Tone Generation

Call progress tones are audible tones sent from switching systems to calling parties (or equipment) to indicate the status of calls. Calling parties can identify the success of a placed call by what is heard after dialing.

The M-991 series utilizes a highly linear tone generator that produces the unique frequencies (singly or in pairs) that are common to call progress signals. Duration and frequency selection are digitally controlled (see Table 2 for data settings for a particular tone output). A typical control sequence for the M-991 is: (1) set data lines to desired frequency selection, (2) wait for data lines to settle, (3) drive the chip enable ($\overline{CE}$) low, (4) maintain $\overline{CE}$ low for desired tone duration (Note: data lines may be changed after data hold time), and (4) return $\overline{CE}$ to a logic high. (Commonly used call progress tones are shown in Table 2.)

In a bus-oriented system, noise on the data lines may propagate through the device and appear at the output. To safeguard against this, use an external latch to lock the data into the device. In addition, it is good practice to bypass the V_{REF} pin to ground with a small capacitor (≈0.01 µF) to reduce power supply

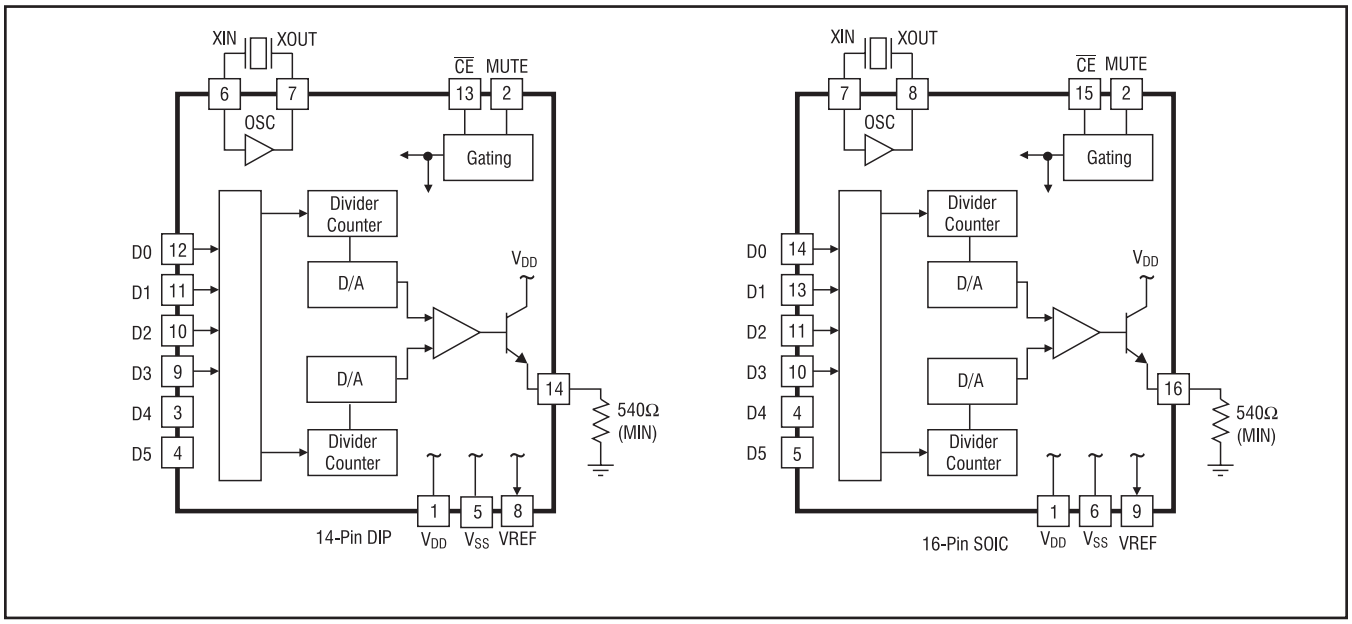


Figure 2 Block Diagrams

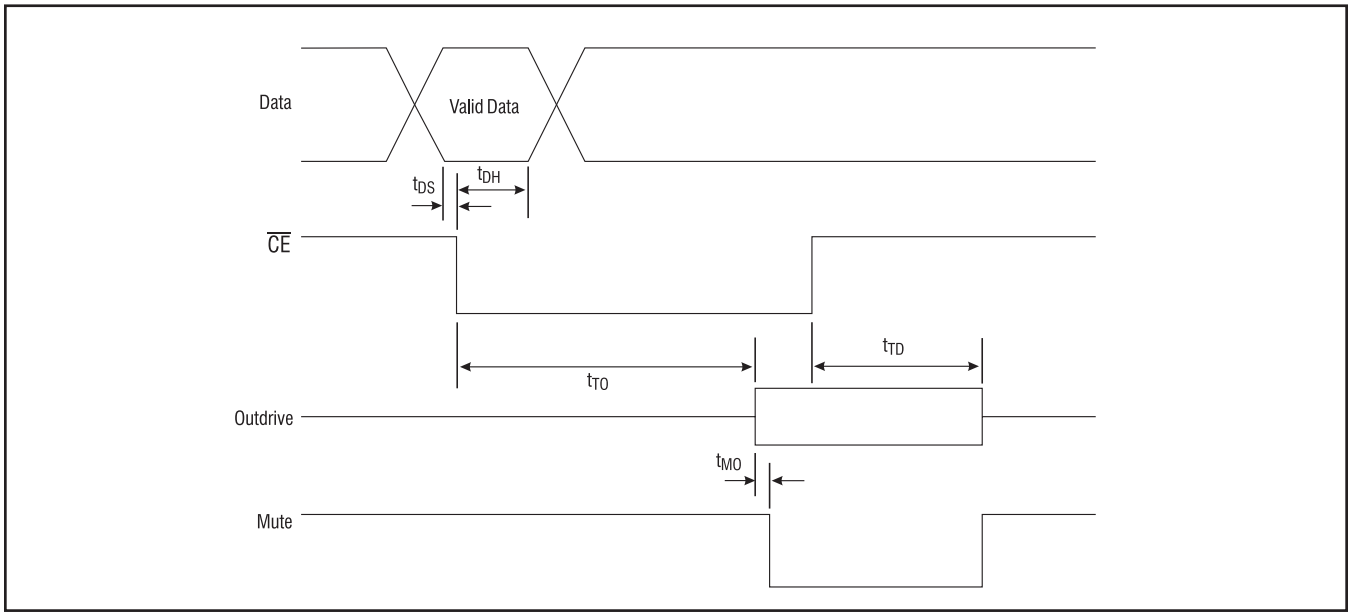


Figure 3 Timing Diagram

noise. The designer should be aware of device timing requirements and design accordingly. The data input pins may be tied high (+5 VDC) or low (ground) as required, but D4 and D5 must be left open. Beware of hardwiring the $\overline{CE}$ pin for dedicated tone generation. This input is edge triggered. An RC network like that shown in Figure 4 should be used to momentarily reset the device immediately following power-up to ensure proper operation.

Ordering Information:

M-991	14-pin plastic DIP
M-991-01SM	16-pin SOIC
M-991-01SMTR	16-pin SOIC Tape and Reel
M-991-02SM	16-pin SOIC, Extended Temperature Range
M-991-02SMTR	16-pin SOIC, Extended Temperature Range, Tape and Reel

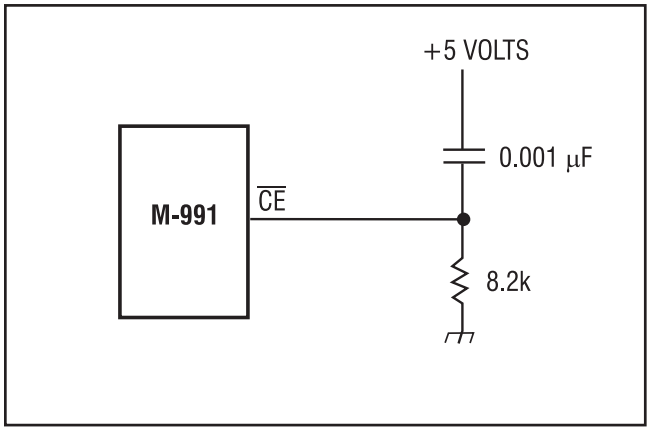


Figure 4 Power-on Reset Circuit

Table 1 Pin Functions

Pin	Function
CE	Latches data and enables output (active low input).
D0 - D3	Data input ins. (See Table 2.)
D4-D5	Leave open.
MUTE	Output indicates that a signal is being generated at OUTDRIVE.
OUTDRIVE	Linear buffered tone output.
V_{DD}	Most positive power supply input pin.
VREF	Internally generated mid-power supply voltage (output).
V_{SS}	Most negative power supply input pin.
XIN	Crystal oscillator or digital clock input.
XOUT	Crystal oscillator output.

Table 2 Data/Tone Selection

D3	D2	D1	D0	Frequency (Hz) 1	Frequency (Hz) 2	Use
0	0	0	0	350	440	Dial Tone
0	0	0	1	400	Off	Special
0	0	1	0	440	Off	Alert Tone
0	0	1	1	440	480	Audible Ring
0	1	0	0	440	620	Pre-empt
0	1	0	1	480	Off	Bell high tone
0	1	1	0	480	620	Reorder (Bell low)
0	1	1	1	350	Off	Special
1	0	0	0	620	Off	Special
1	0	0	1	941	1209	DTMF “*”

Table 3 Standard Call Progress Tones

Tone Name	Frequency (Hz) 1	2	Interruption Rate
Dial	350	440	Steady
Reorder	480	620	Repeat, tones on and off 250 ms ± 25 ms each.
Busy	480	620	Repeat, tones on and off 500 ms ± 50 ms each.
Audible Ring	440	480	Reat, tones on 2 ± 0.2 s, tones off 4 ± 0.4 s
Recall Dial	350	440	Three bursts tones on and off 100 ms ± 20 ms each followed by dail tone.
Special AR	440	480	Tones on 1 ± 0.2s, followed by single 440 Hz on for 0.2s on, and silence for 3 ± 0.3 s, repeat.
Intercept	440	620	Repeat alternating tones, each on for 230 ms ± 70 ms with total cycle of 500 ± 50 ms.
Call Waiting	440	Off	One burst 200 ± 100 ms
Busy Verification	440	Off	One burst of tone on 1.75 ± 0.25 s before attendant intrudes, followed by burst of tone 0.65 ± 0.15 s on, 8 to 20 s apart for as long as the call lasts
Executive Override	440	Off	One burst of tone for 3 ± 1 s before overriding station intrudes
Confirmation	350	440	Three bursts on and off 100 ms each or 100 ms on, 100 ms off, 300 ms on

Table 4 Absolute Maximum Ratings

Storage Temperature	-55° to 125° C
Operating Ambient Temperature	-25° to 70° C
Operating Ambient Temperature for the M-991-02SM	-40° to 85° C
V_{DD}	7.0V
Any Input Voltage	V_{SS} -0.6 to V_{DD} +0.6V

Note:
1. Exceeding these ratings may permanently damage the M-991.

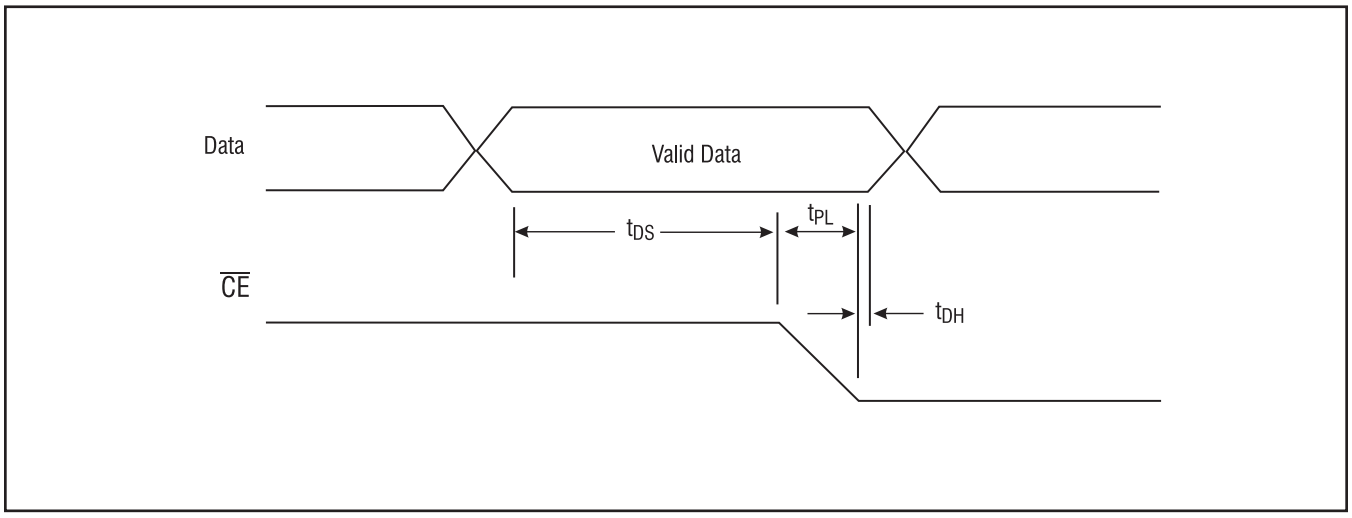


Figure 5 Expanded Wire Data Timing Diagram

Table 5 Specifications

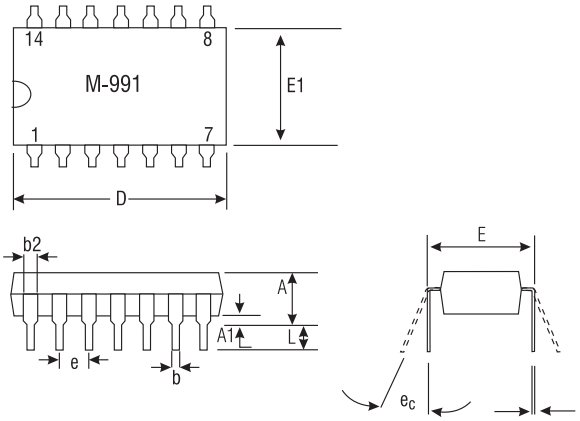
PARAMETER		MIN	TYP	MAX	UNITS	NOTES
Power Supply and Reference	V_{DD}	4.75	—	5.25	V	1
	Current Drain, IDD	—	2.0/4.0		mA	8
	V_{REF} Pin:					
	Deviation from $(V_{DD} + V_{SS})/2$	-2	—	+2	%	
	Internal Resistance from V_{REF} to V_{DD}, V_{SS}	3.25	—	6.75	kΩ	
Oscillator	Frequency Deviation	-0.01	—	+0.01	%	7
	External Clock: (XOUT open)					
	V_{IL}	0	—	0.2	V	
	V_{IH}	V_{DD} - 0.2	—	V_{DD}	V	
	Duty Cycle	40	—	60	%	
	XIN, XOUT Loading:					
	Capacitance	—	—	10	pF	10
	Resistance	20	—	—	MΩ	
Tone Output	Frequency Deviation	-0.5	—	+0.5	%	
	Level	100	—	180	mV	2
	Distorting Components	-35	—	—	dB	3
	Idle	—	—	-60	dBm	4
	OUTDRIVE Envelope Rise Time	—	—	4	ms	5
Control	DX, $\overline{CE}$ Pns:					6
	V_{IL}	—	—	0.5	V	
	V_{IH}	2.5	—	—	V	
	Mute Pins:					
	V_{OL} (I_{SINK} = -100 μA)	—	—	1.5	V	
	V_{OH} (I_{SOURCE} = 100 μA)	V_{DD} - 1.5	—	—	V	
Timing	Data Setup (t_{DS})	200	—	—	ns	11
	Data Hold (t_{DH})	10	—	—	ns	
	Chip Enable Fall (t_{PL})	—	—	90	ns	
	Tone On Delay (tTO)	—	—	5	ms	
	Tone Off Delay (t_{TD})	—	—	5	ms	
	Mute Delay from Outdrive (t_{MO})	—	—	200	ns	

Notes: (unless otherwise specified)

1. All DC voltages are referenced to V_{SS}.
2. Vrms per tone, 540 Ω load.
3. Any one frequency relative to the lowest level output tone (f<4000 Hz).
4. 0 dBm = 0.775 Vrms.
5. To 90% maximum amplitude.
6. For all supply voltages in the operating range.
7. At XOUT pin as compared to 3.579545 MHz.
8. OUTDRIVE with load >5 KΩ/OUTDRIVE with 540 Ω load.
9. Resistance at V_{REF} to V_{DD} or V_{SS} > 1 MΩ.
10. Crystal oscillator active.
11. Measured 90% to 10%.

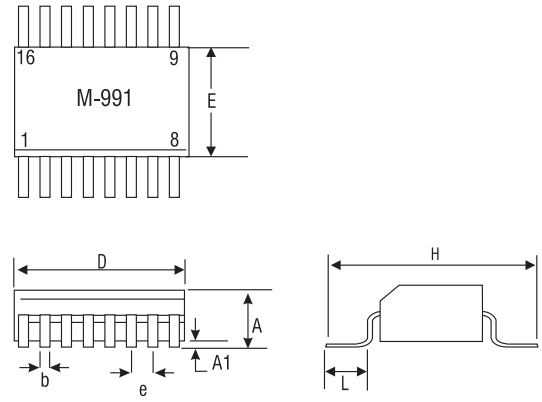
Drawing not to scale.
Does not reflect actual part marking.

14-Pin DIP



Tolerances				
	Inches		Metric (mm)	
	Min	Max	Min	Max
A		.210		5.33
A1	.015		.38	
b	.014	.022	.36	.56
b2	.045	.070	1.1	1.8
C	.008	.014	.20	.36
D	.735	.775	18.7	19.7
E	.300	.325	7.6	8.3
E1	.240	.280	6.1	7.1
e	.100 BSC		2.54 BSC	
ec	0°	15°	0°	15°
L	.115	.150	2.9	4.1

16-Pin SOIC



Tolerances				
	(Inches)		Metric (mm)	
	Min	Max	Min	Max
A	.0926	.1043	2.35	2.65
A1	.0040	.0118	.10	.30
b	.013	.020	.33	.51
D	.3977	.4133	10.10	10.50
E	.2914	.2992	7.4	7.6
e	.050 BSC		1.27 BSC	
H	.394	.419	10.00	10.65
L	.016	.050	.40	1.27

Figure 6 Package Dimensions

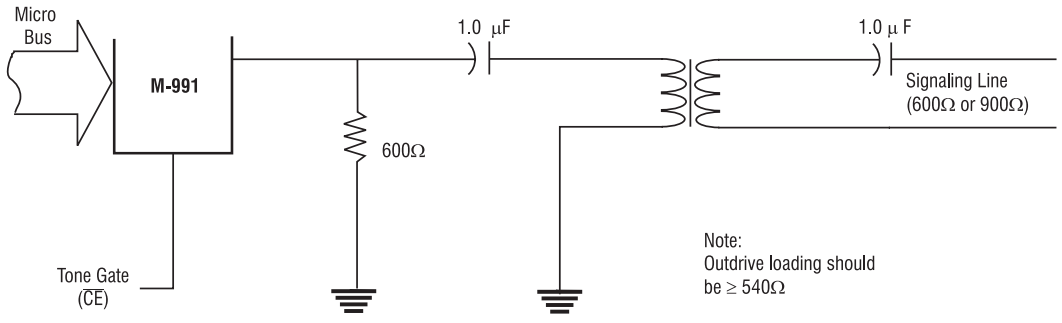


Figure 7 Typical Application