

256K-BIT CMOS STATIC RAM
 32K-WORD BY 8-BIT

Jameco Part Number 41988

Description

The μ PD43256B is a high speed, low power, and 262, 144 bits (32,768 words by 8 bits) CMOS static RAM. Battery backup is available (L, LL, A, and B versions). And A and B versions are wide voltage operations. The μ PD43256B is packed in 28-pin plastic DIP, 28-pin plastic SOP and 28-pin plastic TSOP (I).

Features

- 32,768 words by 8 bits organization
- Fast access time: 70, 85, 100, 120, 150 ns (MAX.)
- Wide voltage range (A version: $V_{cc} = 3.0$ to 5.5 V, B version: $V_{cc} = 2.7$ to 5.5 V)
- 2 V data retention
- OE input for easy application

| Part number | Access time ns (MAX.) | Operating supply voltage V | Operating temperature °C | Standby supply current μ A (MAX.) | Data retention supply current ^{Note 1} μ A (MAX.) |
|--------------------------------------|---|----------------------------|--------------------------|---------------------------------------|--|
| μ PD43256B-L | 70, 85 | 4.5 to 5.5 | 0 to 70 | 50 | 3 |
| μ PD43256B-LL | 70, 85 | | | 15 | 2 |
| ★ μ PD43256B-A | 85, 100 ^{Note 2} , 120 ^{Note 2} | 3.0 to 5.5 | | | |
| ★ μ PD43256B-B ^{Note 2} | 100, 120, 150 | 2.7 to 5.5 | | | |

- Notes** 1. $T_A \leq 40$ °C, $V_{cc} = 3$ V
 2. Access time : 85 ns (MAX.) ($V_{cc} = 4.5$ to 5.5 V)

Version X and P

This data sheet can be applied to the version X and P. Each version is identified with its lot number. Letter X in the fifth character position in a lot number signifies version X, letter P, version P.



The information in this document is subject to change without notice.

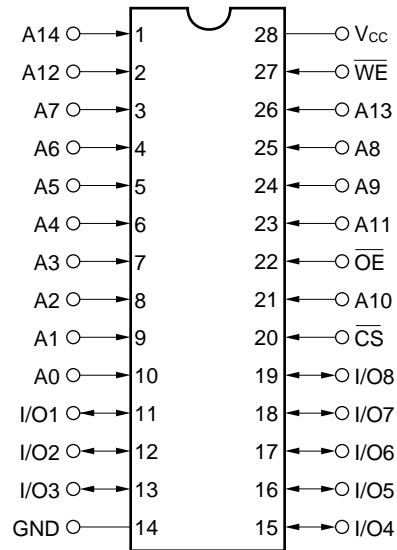
Ordering Information

| Part number | Package | Access time ns (MAX.) | Operating supply voltage V | Operating temperature °C | Remark |
|----------------------|---|--|----------------------------------|--------------------------------|------------|
| μPD43256BCZ-70L | 28-pin plastic DIP (600 mil) | 70 | 4.5 to 5.5 | 0 to 70 | L Version |
| μPD43256BCZ-85L | | 85 | | | LL Version |
| μPD43256BCZ-70LL | | 70 | | | |
| μPD43256BCZ-85LL | | 85 | | | |
| μPD43256BGU-70L | 28-pin plastic SOP (450 mil) | 70 | 3.0 to 5.5 | | L Version |
| μPD43256BGU-85L | | 85 | | | |
| μPD43256BGU-70LL | | 70 | | | LL Version |
| μPD43256BGU-85LL | | 85 | | | |
| μPD43256BGU-A85 | | 85 | A Version | | |
| μPD43256BGU-A10 | | 100 | | | |
| μPD43256BGU-A12 | | 120 | | | |
| μPD43256BGU-B10 | | 100 | 2.7 to 5.5 | | B Version |
| μPD43256BGU-B12 | | 120 | | | |
| μPD43256BGU-B15 | | 150 | | | |
| μPD43256BGW-70LL-9JL | | 28-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent) | 70 | | 4.5 to 5.5 |
| μPD43256BGW-85LL-9JL | 85 | | | | |
| μPD43256BGW-A85-9JL | 85 | | 3.0 to 5.5 | A Version | |
| μPD43256BGW-A10-9JL | 100 | | | | |
| μPD43256BGW-A12-9JL | 120 | | | | |
| μPD43256BGW-B10-9JL | 100 | | 2.7 to 5.5 | B Version | |
| μPD43256BGW-B12-9JL | 120 | | | | |
| μPD43256BGW-B15-9JL | 150 | | | | |
| μPD43256BGW-70LL-9KL | 28-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent) | 70 | 4.5 to 5.5 | LL Version | |
| μPD43256BGW-85LL-9KL | | 85 | | | |
| μPD43256BGW-A85-9KL | | 85 | 3.0 to 5.5 | A Version | |
| μPD43256BGW-A10-9KL | | 100 | | | |
| μPD43256BGW-A12-9KL | | 120 | | | |
| μPD43256BGW-B10-9KL | | 100 | 2.7 to 5.5 | B Version | |
| μPD43256BGW-B12-9KL | | 120 | | | |
| μPD43256BGW-B15-9KL | | 150 | | | |

Pin Configuration (Marking Side)

28-pin plastic DIP (600 mil)
 μPD43256BCZ

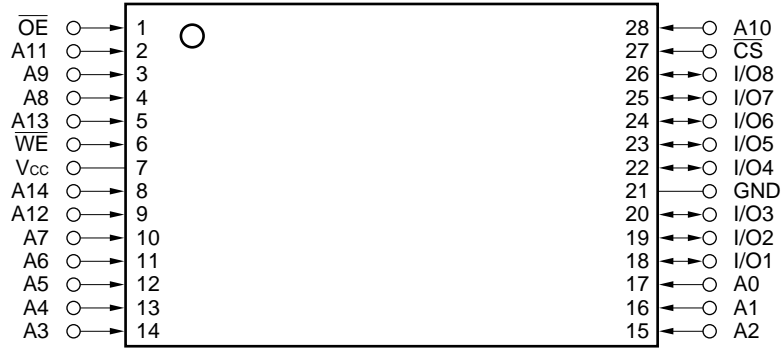
28-pin plastic SOP (450 mil)
 μPD43256BGU



- A0 - A14 : Address inputs
- I/O1 - I/O8 : Data inputs/outputs
- CS : Chip Select
- WE : Write Enable
- OE : Output Enable
- V_{CC} : Power supply
- GND : Ground

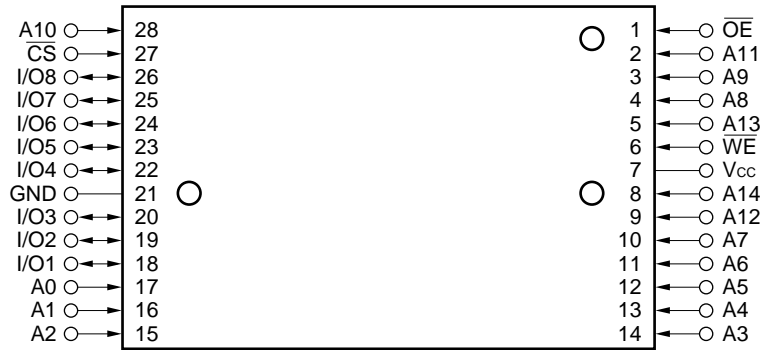
28-pin plastic TSOP (I) (8 × 13.4 mm)
(Normal bent)

μPD43256BGW-9JL

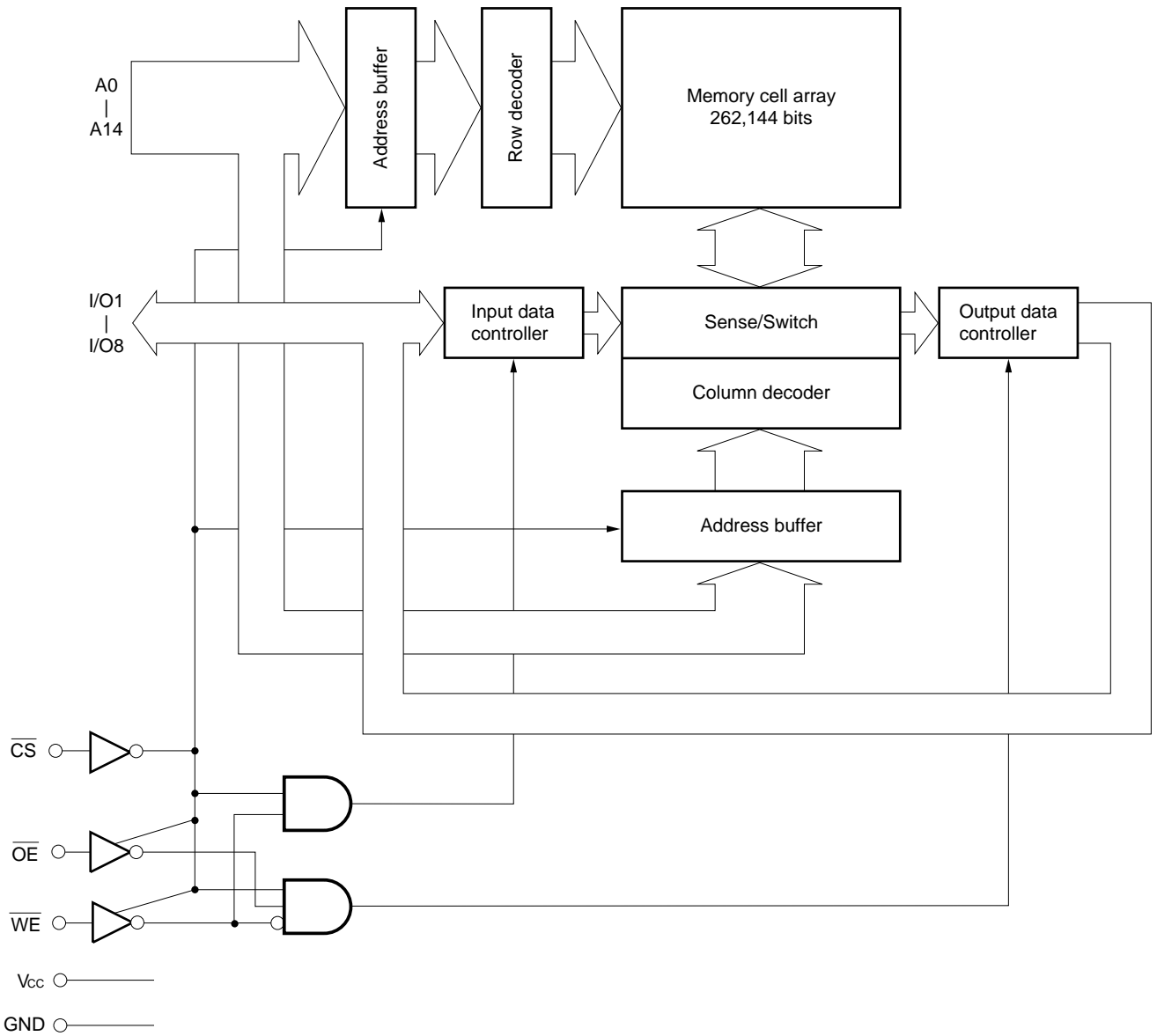


28-pin plastic TSOP (I) (8 × 13.4 mm)
(Reverse bent)

μPD43256BGW-9KL



Block Diagram



Truth Table

| \overline{CS} | \overline{OE} | \overline{WE} | Mode | I/O | Supply current |
|-----------------|-----------------|-----------------|----------------|------------------|----------------|
| H | × | × | Not selected | High impedance | I_{SB} |
| L | H | H | Output disable | | I_{CCA} |
| L | × | L | Write | D _{IN} | I_{CCA} |
| L | L | H | Read | D _{OUT} | |

Remark ×: Don't care

Electrical Characteristics

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|-------------------------------|------------------|---|------|
| Supply voltage | V _{CC} | -0.5 ^{Note} to +7.0 | V |
| Input/Output voltage | V _I | -0.5 ^{Note} to V _{CC} + 0.5 | V |
| Operating ambient temperature | T _A | 0 to 70 | °C |
| Storage temperature | T _{stg} | -55 to +125 | °C |

Note -3.0 V (MIN.) (Pulse width 50 ns)

Caution Exposing the device to stress above those listed in absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this characteristics. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

| Parameter | Symbol | μPD43256B-L μPD43256B-LL | | μPD43256B-A | | μPD43256B-B | | Unit |
|-------------------------------|-----------------|-----------------------------|-----------------------|----------------------|-----------------------|----------------------|-----------------------|------|
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | |
| Supply voltage | V _{CC} | 4.5 | 5.5 | 3.0 | 5.5 | 2.7 | 5.5 | V |
| High level input voltage | V _{IH} | 2.2 | V _{CC} + 0.5 | 2.2 | V _{CC} + 0.5 | 2.2 | V _{CC} + 0.5 | V |
| Low level input voltage | V _{IL} | -0.3 ^{Note} | +0.8 | -0.3 ^{Note} | +0.5 | -0.3 ^{Note} | +0.5 | V |
| Operating ambient temperature | T _A | 0 | 70 | 0 | 70 | 0 | 70 | °C |

Note -3.0 V (MIN.) (Pulse width 50 ns)

DC Characteristics (Recommended operating conditions unless otherwise noted) (1/2)

| Parameter | Symbol | Test conditions | μPD43256B-L | | | μPD43256B-LL | | | Unit |
|---------------------------|-------------------|---|----------------------|------|------|----------------------|------|------|------|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | |
| Input leakage current | I _{LI} | V _{IN} = 0 V to V _{CC} | -1.0 | | +1.0 | -1.0 | | +1.0 | μA |
| I/O leakage current | I _{LO} | V _{I/O} = 0 V to V _{CC} $\overline{OE} = V_{IH}$ or $\overline{CS} = V_{IH}$ or $\overline{WE} = V_{IL}$ | -1.0 | | +1.0 | -1.0 | | +1.0 | μA |
| Operating supply current | I _{CCA1} | $\overline{CS} = V_{IL}$, Minimum cycle time, I _{I/O} = 0 mA | | | 45 | | | 45 | mA |
| | I _{CCA2} | $\overline{CS} = V_{IL}$, I _{I/O} = 0 mA | | | 10 | | | 10 | |
| | I _{CCA3} | $\overline{CS} \leq 0.2$ V, Cycle = 1 MHz, I _{I/O} = 0 mA V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V | | | 10 | | | 10 | |
| Standby supply current | I _{SB} | $\overline{CS} = V_{IH}$ | | | 3 | | | 3 | mA |
| | I _{SB1} | $\overline{CS} \geq V_{CC} - 0.2$ V | | 1.0 | 50 | | 0.5 | 15 | |
| High level output voltage | V _{OH1} | I _{OH} = -1.0 mA | 2.4 | | | 2.4 | | | V |
| | V _{OH2} | I _{OH} = -0.1 mA | V _{CC} -0.5 | | | V _{CC} -0.5 | | | |
| Low level output voltage | V _{OL} | I _{OL} = 2.1 mA | | | 0.4 | | | 0.4 | V |

Remarks 1. V_{IN}: Input voltage

2. These DC Characteristics are in common regardless of package types.

DC Characteristics (Recommended operating conditions unless otherwise noted) (2/2)

| Parameter | Symbol | Test conditions | μPD43256B-A | | | μPD43256B-B | | | Unit | |
|----------------------------|--|---|--|------|------|----------------------|------|------|------|----|
| | | | MIN. | TYP. | MAX. | MIN. | TYP. | MAX. | | |
| Input leakage current | I _{LI} | V _{IN} = 0 V to V _{CC} | -1.0 | | +1.0 | -1.0 | | +1.0 | μA | |
| I/O leakage current | I _{LO} | V _{I/O} = 0 V to V _{CC} CS = V _{IH} or WE = V _{IL} or OE = V _{IH} | -1.0 | | +1.0 | -1.0 | | +1.0 | μA | |
| ★ Operating supply current | I _{CCA1} | CS = V _{IL} , Minimum cycle time, I _{I/O} = 0 mA | μPD43256B-A85 | | | 45 | | | — | mA |
| | | | μPD43256B-A10 | | | | | | | |
| | | | μPD43256B-A12 | | | | | | | |
| | | | μPD43256B-B10 | | | — | | | | |
| | | | μPD43256B-B12 | | | 45 | | | | |
| | μPD43256B-B15 | | | — | | | | | | |
| V _{CC} ≤ 3.3 V | | | — | | | 20 | | | | |
| I _{CCA2} | CS = V _{IL} , I _{I/O} = 0 mA | | | | 10 | | | 10 | | |
| | | V _{CC} ≤ 3.3 V | | | — | | | 5 | | |
| I _{CCA3} | CS ≤ 0.2 V, Cycle = 1 MHz, I _{I/O} = 0 mA, V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V | | | | 10 | | | 10 | | |
| | | V _{CC} ≤ 3.3 V | | | — | | | 5 | | |
| Standby supply current | I _{SB} | CS = V _{IH} | | | | 3 | | | 3 | |
| | | | V _{CC} ≤ 3.3 V | | | — | | | 2 | |
| I _{SB1} | CS ≥ V _{CC} - 0.2 V | | | | 0.5 | | | 15 | | |
| | | V _{CC} ≤ 3.3 V | | | — | | | 0.5 | | 10 |
| High level output voltage | V _{OH1} | I _{OH} = -1.0 mA, V _{CC} ≥ 4.5 V | 2.4 | | | 2.4 | | | V | |
| | | | I _{OH} = -0.5 mA, V _{CC} < 4.5 V | | | 2.4 | | | | |
| | V _{OH2} | I _{OH} = -0.1 mA | — | | | — | | | | |
| | | | I _{OH} = -0.02 mA | | | V _{CC} -0.1 | | | | |
| Low level output voltage | V _{OL} | I _{OL} = 2.1 mA, V _{CC} ≥ 4.5 V | | | | 0.4 | | | 0.4 | |
| | | | I _{OL} = 1.0 mA, V _{CC} < 4.5 V | | | | | | 0.4 | |
| | V _{OL1} | I _{OL} = 0.02 mA | | | | 0.1 | | | 0.1 | |

- Remarks 1. V_{IN}: Input voltage
 2. These DC characteristics are in common regardless of package types.

Capacitance (T_A = 25 °C, f = 1 MHz)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|--------------------------|------------------|------------------------|------|------|------|------|
| Input capacitance | C _{IN} | V _{IN} = 0 V | | | 5 | pF |
| Input/Output capacitance | C _{I/O} | V _{I/O} = 0 V | | | 8 | pF |

- Remarks 1. V_{IN}: Input voltage
 2. These parameters are periodically sampled and not 100 % tested.

AC Characteristics (Recommended operating conditions unless otherwise noted)

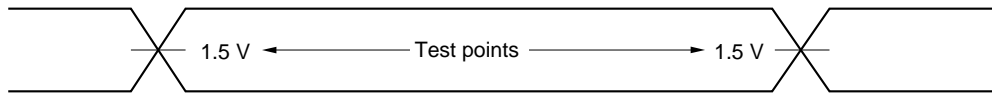
AC Test Conditions

Input waveform (Rise/fall time \leq 5 ns)

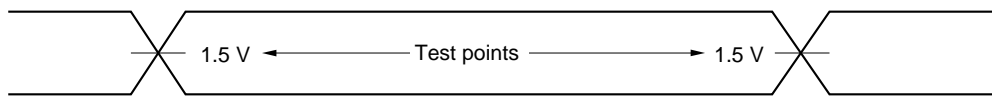
Input pulse levels

0.8 V to 2.2 V: μ PD43256B-L, 43256B-LL

0.5 V to 2.2 V: μ PD43256B-A, 43256B-B



Output waveform



Output load

μ PD43256B-A, 43256B-B: 1TTL + 100 pF

μ PD43256B-L, 43256B-LL:

AC characteristics with notes should be measured with the output load shown in

Figure 1 and **Figure 2**.

Figure 1

(For t_{AA} , t_{ACS} , t_{OE} , t_{OH})

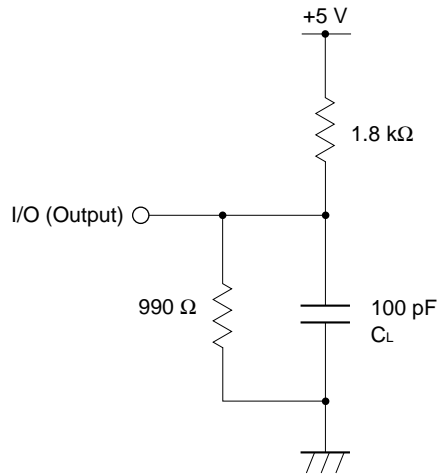
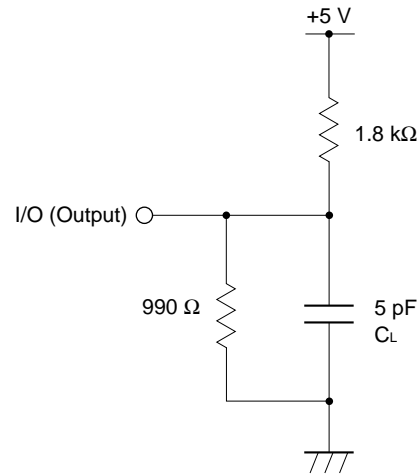


Figure 2

(For t_{CHZ} , t_{CLZ} , t_{OHZ} , t_{OLZ} , t_{WHZ} , t_{OW})



Remark C_L includes capacitances of the probe and jig, and stray capacitances.

★ Read Cycle (1/2)

| Parameter | Symbol | V _{CC} ≥ 4.5 V | | | | Unit | Condition |
|--|------------------|-------------------------|------|--|------|------|-----------|
| | | μPD43256B-70 | | μPD43256B-85 μPD43256B-A85/A10/A12 μPD43256B-B10/B12/B15 | | | |
| | | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t _{RC} | 70 | | 85 | | ns | |
| Address access time | t _{AA} | | 70 | | 85 | ns | Note 1 |
| $\overline{\text{CS}}$ access time | t _{ACS} | | 70 | | 85 | ns | |
| $\overline{\text{OE}}$ access time | t _{OE} | | 35 | | 40 | ns | |
| Output hold from address change | t _{OH} | 10 | | 10 | | ns | |
| $\overline{\text{CS}}$ to output in low impedance | t _{CLZ} | 10 | | 10 | | ns | Note 2 |
| $\overline{\text{OE}}$ to output in low impedance | t _{OLZ} | 5 | | 5 | | ns | |
| $\overline{\text{CS}}$ to output in high impedance | t _{CHZ} | | 30 | | 30 | ns | |
| $\overline{\text{OE}}$ to output in high impedance | t _{OHZ} | | 30 | | 30 | ns | |

- Notes** 1. See the output load shown in **Figure 1** except for μPD43256B-A, 43256B-B.
 2. See the output load shown in **Figure 2** except for μPD43256B-A, 43256B-B.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

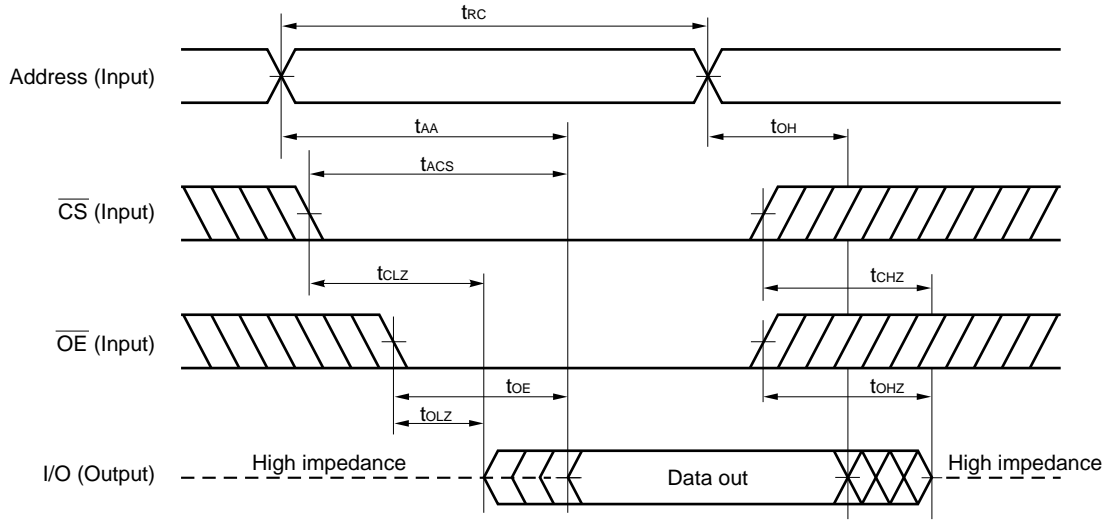
★ Read Cycle (2/2)

| Parameter | Symbol | V _{CC} ≥ 3.0 V | | | | | | V _{CC} ≥ 2.7 V | | | | | | Unit | Con- dition |
|--|------------------|-------------------------|------|---------------|------|---------------|------|-------------------------|------|---------------|------|---------------|------|------|----------------|
| | | μPD43256B-A85 | | μPD43256B-A10 | | μPD43256B-A12 | | μPD43256B-B10 | | μPD43256B-B12 | | μPD43256B-B15 | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Read cycle time | t _{RC} | 85 | | 100 | | 120 | | 100 | | 120 | | 150 | | ns | |
| Address access time | t _{AA} | | 85 | | 100 | | 120 | | 100 | | 120 | | 150 | ns | Note |
| $\overline{\text{CS}}$ access time | t _{ACS} | | 85 | | 100 | | 120 | | 100 | | 120 | | 150 | ns | |
| $\overline{\text{OE}}$ access time | t _{OE} | | 50 | | 60 | | 60 | | 60 | | 60 | | 70 | ns | |
| Output hold from address change | t _{OH} | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{\text{CS}}$ to output in low impedance | t _{CLZ} | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | ns | |
| $\overline{\text{OE}}$ to output in low impedance | t _{OLZ} | 5 | | 5 | | 5 | | 5 | | 5 | | 5 | | ns | |
| $\overline{\text{CS}}$ to output in high impedance | t _{CHZ} | | 35 | | 35 | | 40 | | 35 | | 40 | | 50 | ns | |
| $\overline{\text{OE}}$ to output in high impedance | t _{OHZ} | | 35 | | 35 | | 40 | | 35 | | 40 | | 50 | ns | |

Note Loading condition is 1TTL + 100 pF.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

Read Cycle Timing Chart



Remark In read cycle, \overline{WE} should be fixed to high level.

★ Write Cycle (1/2)

| Parameter | Symbol | V _{CC} ≥ 4.5 V | | | | Unit | Condition |
|--|------------------|-------------------------|------|--|------|------|-----------|
| | | μPD43256B-70 | | μPD43256B-85 μPD43256B-A85/A10/A12 μPD43256B-B10/B12/B15 | | | |
| | | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | t _{WC} | 70 | | 85 | | ns | |
| $\overline{\text{CS}}$ to end of write | t _{CW} | 50 | | 70 | | ns | |
| Address valid to end of write | t _{AW} | 50 | | 70 | | ns | |
| Write pulse width | t _{WP} | 55 | | 60 | | ns | |
| Data valid to end of write | t _{DW} | 30 | | 35 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | ns | |
| Write recovery time | t _{WR} | 0 | | 0 | | ns | |
| $\overline{\text{WE}}$ to output in high impedance | t _{WHZ} | | 30 | | 30 | ns | Note |
| Output active from end of write | t _{OW} | 10 | | 10 | | ns | |

Note See the output load shown in **Figure 2** except for μPD43256B-A, 43256B-B.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

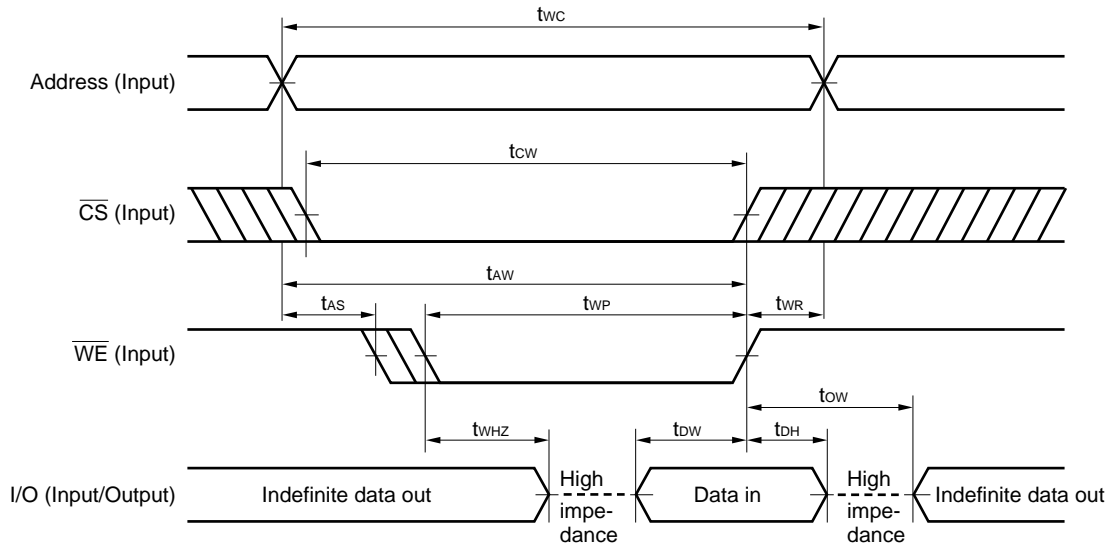
★ Write Cycle (2/2)

| Parameter | Symbol | V _{CC} ≥ 3.0 V | | | | | | V _{CC} ≥ 2.7 V | | | | | | Unit | Con- dition |
|--|------------------|-------------------------|------|---------------|------|---------------|------|-------------------------|------|---------------|------|---------------|------|------|----------------|
| | | μPD43256B-A85 | | μPD43256B-A10 | | μPD43256B-A12 | | μPD43256B-B10 | | μPD43256B-B12 | | μPD43256B-B15 | | | |
| | | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | MIN. | MAX. | | |
| Write cycle time | t _{WC} | 85 | | 100 | | 120 | | 100 | | 120 | | 150 | | ns | |
| $\overline{\text{CS}}$ to end of write | t _{CW} | 70 | | 70 | | 90 | | 70 | | 90 | | 100 | | ns | |
| Address valid to end of write | t _{AW} | 70 | | 70 | | 90 | | 70 | | 90 | | 100 | | ns | |
| Write pulse width | t _{WP} | 60 | | 60 | | 80 | | 60 | | 80 | | 90 | | ns | |
| Data valid to end of write | t _{DW} | 60 | | 60 | | 70 | | 60 | | 70 | | 80 | | ns | |
| Data hold time | t _{DH} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Address setup time | t _{AS} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| Write recovery time | t _{WR} | 0 | | 0 | | 0 | | 0 | | 0 | | 0 | | ns | |
| $\overline{\text{WE}}$ to output in high impedance | t _{WHZ} | | 30 | | 35 | | 40 | | 35 | | 40 | | 50 | ns | Note |
| Output active from end of write | t _{OW} | 10 | | 10 | | 10 | | 10 | | 10 | | 10 | | ns | |

Note Loading condition is 1TTL + 100 pF.

Remark These AC characteristics are in common regardless of package types and L, LL versions.

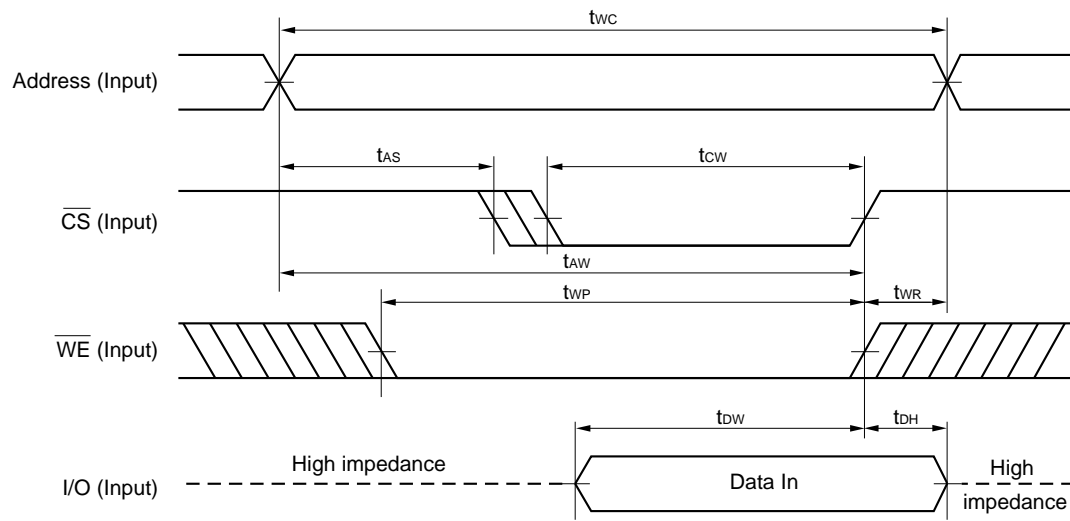
Write Cycle Timing Chart 1 (\overline{WE} Controlled)



- Cautions**
1. \overline{CS} or \overline{WE} should be fixed to high level during address transition.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level \overline{CS} and a low level \overline{WE} .
 2. When \overline{WE} is at low level, the I/O pins are always high impedance. When \overline{WE} is at high level, read operation is executed. Therefore \overline{OE} should be at high level to make the I/O pins high impedance.
 3. If \overline{CS} changes to low level at the same time or after the change of \overline{WE} to low level, the I/O pins will remain high impedance state.

Write Cycle Timing Chart 2 (\overline{CS} Controlled)



- Cautions**
1. \overline{CS} or \overline{WE} should be fixed to high level during address transition.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level \overline{CS} and a low level \overline{WE} .

Low Vcc Data Retention Characteristics

L Version (μ PD43256B-L: $T_A = 0$ to 70 °C)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|---|------|------|--------------------|---------|
| Data retention supply voltage | V_{CCDR} | $\overline{CS} \geq V_{CC} - 0.2$ V | 2.0 | | 5.5 | V |
| Data retention supply current | I_{CCDR} | $V_{CC} = 3.0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V | | 0.5 | 20 ^{Note} | μ A |
| Chip deselection to data retention mode | t_{CDR} | | 0 | | | ns |
| Operation recovery time | t_R | | 5 | | | ms |

Note 3 μ A ($T_A \leq 40$ °C)

LL Version (μ PD43256B-LL: $T_A = 0$ to 70 °C)

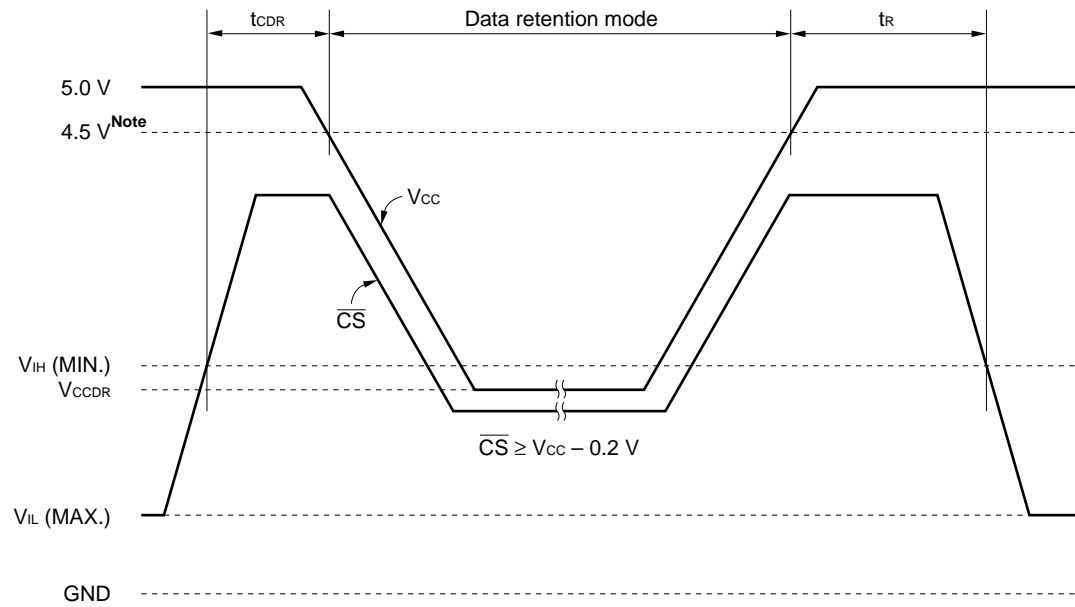
A Version (μ PD43256B-A: $T_A = 0$ to 70 °C)

B Version (μ PD43256B-B: $T_A = 0$ to 70 °C)

| Parameter | Symbol | Test conditions | MIN. | TYP. | MAX. | Unit |
|---|------------|---|------|------|-------------------|---------|
| Data retention supply voltage | V_{CCDR} | $\overline{CS} \geq V_{CC} - 0.2$ V | 2.0 | | 5.5 | V |
| Data retention supply current | I_{CCDR} | $V_{CC} = 3.0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V | | 0.5 | 7 ^{Note} | μ A |
| Chip deselection to data retention mode | t_{CDR} | | 0 | | | ns |
| Operation recovery time | t_R | | 5 | | | ms |

Note 2 μ A ($T_A \leq 40$ °C), 1 μ A ($T_A \leq 25$ °C)

Data Retention Timing Chart

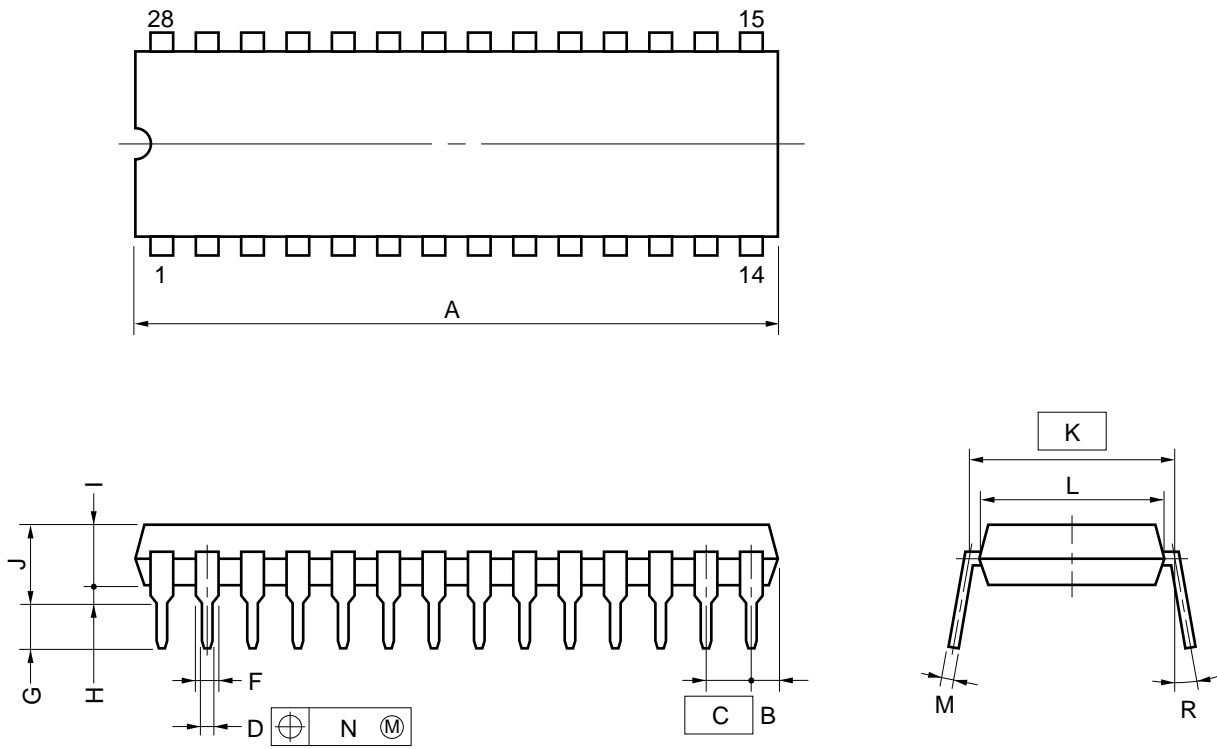


Note A Version: 3.0 V, B Version: 2.7 V

Remark The other pins (address, \overline{OE} , \overline{WE} , I/Os) can be in high impedance state.

Package Drawings

28 PIN PLASTIC DIP (600 mil)



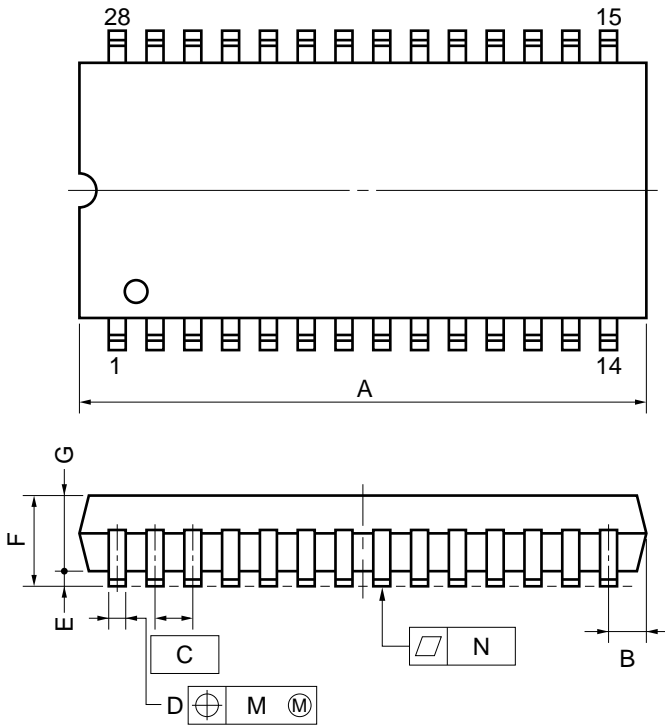
NOTES

- 1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.
- 2) Item "K" to center of leads when formed parallel.

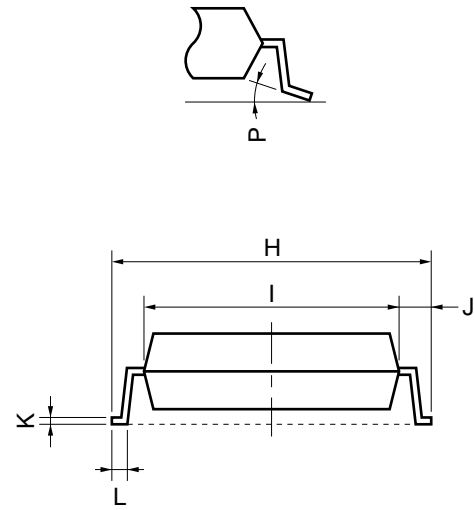
| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 38.10 MAX. | 1.500 MAX. |
| B | 2.54 MAX. | 0.100 MAX. |
| C | 2.54 (T.P.) | 0.100 (T.P.) |
| D | 0.50±0.10 | 0.020 ^{+0.004} _{-0.005} |
| F | 1.2 MIN. | 0.047 MIN. |
| G | 3.6±0.3 | 0.142±0.012 |
| H | 0.51 MIN. | 0.020 MIN. |
| I | 4.31 MAX. | 0.170 MAX. |
| J | 5.72 MAX. | 0.226 MAX. |
| K | 15.24 (T.P.) | 0.600 (T.P.) |
| L | 13.2 | 0.520 |
| M | 0.25 ^{+0.10} _{-0.05} | 0.010 ^{+0.004} _{-0.003} |
| N | 0.25 | 0.01 |
| R | 0 ~ 15° | 0 ~ 15° |

P28C-100-600A1-1

28 PIN PLASTIC SOP (450 mil)



detail of lead end



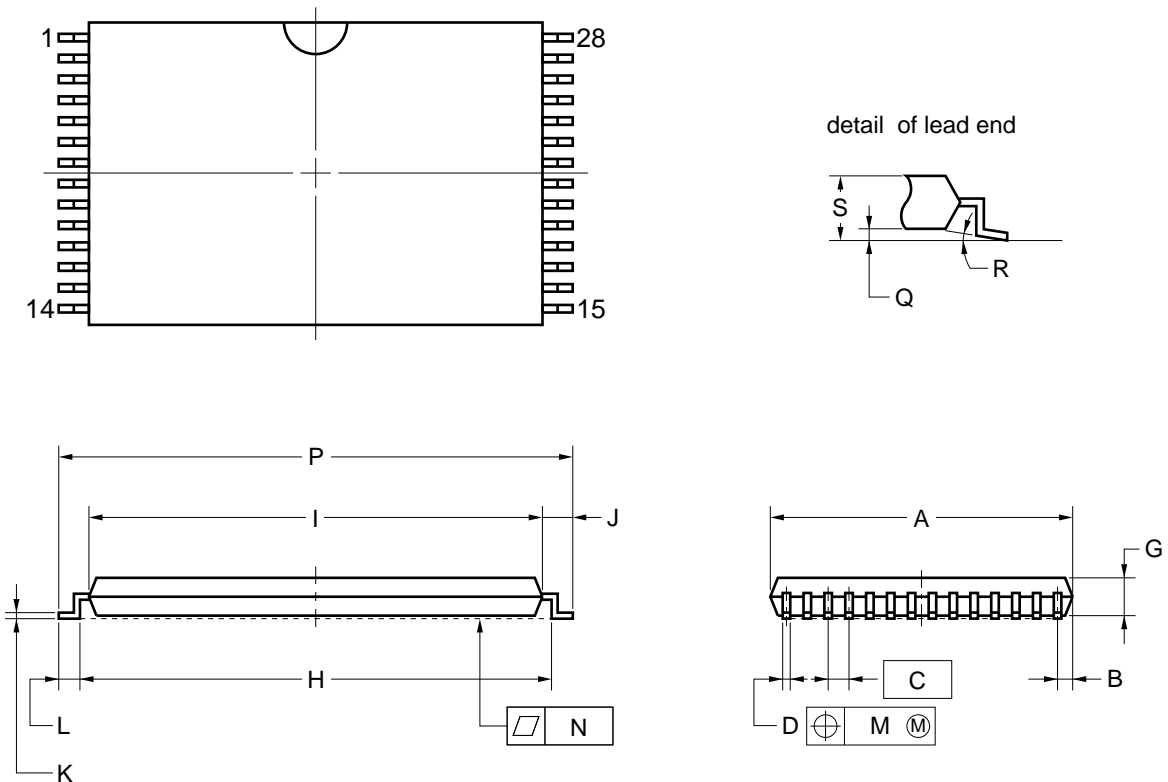
NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS | INCHES |
|------|--|---|
| A | 19.05 MAX. | 0.750 MAX. |
| B | 1.27 MAX. | 0.050 MAX. |
| C | 1.27 (T.P.) | 0.050 (T.P.) |
| D | 0.40±0.10 | 0.016 ^{+0.004} _{-0.005} |
| E | 0.2±0.1 | 0.008±0.004 |
| F | 3.0 MAX. | 0.119 MAX. |
| G | 2.55±0.1 | 0.100 ^{+0.005} _{-0.004} |
| H | 11.8±0.3 | 0.465 ^{+0.012} _{-0.013} |
| I | 8.4±0.1 | 0.331 ^{+0.004} _{-0.005} |
| J | 1.7±0.2 | 0.067±0.008 |
| K | 0.20 ^{+0.07} _{-0.03} | 0.008 ^{+0.003} _{-0.002} |
| L | 0.7±0.2 | 0.028 ^{+0.008} _{-0.009} |
| M | 0.12 | 0.005 |
| N | 0.10 | 0.004 |
| P | 5°±5° | 5°±5° |

P28GU-50-450A-1

28PIN PLASTIC TSOP (I) (8×13.4)



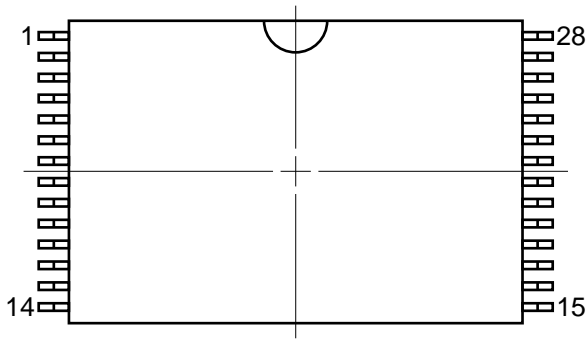
NOTE

- (1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
- (2) "A" excludes mold flash. (Includes mold flash : 8.4mm MAX. <0.331 inch MAX.>)

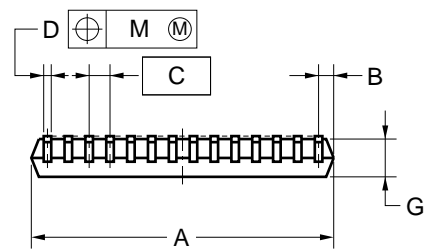
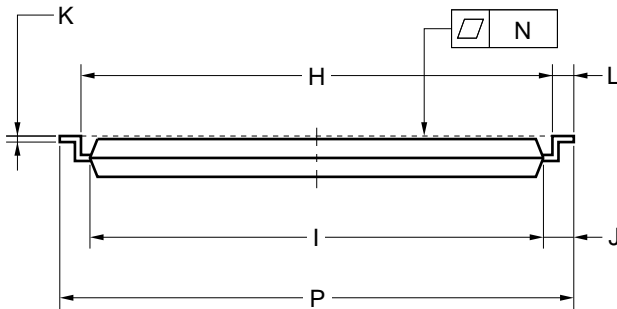
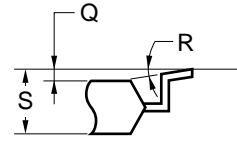
| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 8.0±0.1 | 0.315±0.004 |
| B | 0.6 MAX. | 0.024 MAX. |
| C | 0.55 (T.P.) | 0.022 (T.P.) |
| D | 0.22 ^{+0.08} _{-0.07} | 0.009±0.003 |
| G | 1.0 | 0.039 |
| H | 12.4±0.2 | 0.488±0.008 |
| I | 11.8±0.1 | 0.465 ^{+0.004} _{-0.005} |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.145 ^{+0.025} _{-0.015} | 0.006±0.001 |
| L | 0.5±0.1 | 0.020 ^{+0.004} _{-0.005} |
| M | 0.08 | 0.003 |
| N | 0.10 | 0.004 |
| P | 13.4±0.2 | 0.528 ^{+0.008} _{-0.009} |
| Q | 0.1±0.05 | 0.004±0.002 |
| R | 3° ^{+7°} _{-3°} | 3° ^{+7°} _{-3°} |
| S | 1.2 MAX. | 0.048 MAX. |

P28GW-55-9JL-1

28PIN PLASTIC TSOP (I) (8×13.4)



detail of lead end



NOTE

- (1) Each lead centerline is located within 0.08 mm (0.003 inch) of its true position (T.P.) at maximum material condition.
- (2) "A" excludes mold flash. (Includes mold flash : 8.4mm MAX. <0.331 inch MAX.>)

| ITEM | MILLIMETERS | INCHES |
|------|---|---|
| A | 8.0±0.1 | 0.315±0.004 |
| B | 0.6 MAX. | 0.024 MAX. |
| C | 0.55 (T.P.) | 0.022 (T.P.) |
| D | 0.22 ^{+0.08} _{-0.07} | 0.009±0.003 |
| G | 1.0 | 0.039 |
| H | 12.4±0.2 | 0.488±0.008 |
| I | 11.8±0.1 | 0.465 ^{+0.004} _{-0.005} |
| J | 0.8±0.2 | 0.031 ^{+0.009} _{-0.008} |
| K | 0.145 ^{+0.025} _{-0.015} | 0.006±0.001 |
| L | 0.5±0.1 | 0.020 ^{+0.004} _{-0.005} |
| M | 0.08 | 0.003 |
| N | 0.10 | 0.004 |
| P | 13.4±0.2 | 0.528 ^{+0.008} _{-0.009} |
| Q | 0.1±0.05 | 0.004±0.002 |
| R | 3° ^{+7°} _{-3°} | 3° ^{+7°} _{-3°} |
| S | 1.2 MAX. | 0.048 MAX. |

P28GW-55-9KL-1

Recommended Soldering Conditions

The following conditions (See table below) must be met when soldering μPD43256B. For more details, refer to our document “**SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL**” (C10535E).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Types of Surface Mount Device

μPD43256BGU: 28-pin plastic SOP (450 mil)

μPD43256BGW-9JL: 28-pin plastic TSOP (I) (8 × 13.4 mm) (Normal bent)

μPD43256BGW-9KL: 28-pin plastic TSOP (I) (8 × 13.4 mm) (Reverse bent)

Please consult with our sales offices.

Type of Through Hole Mount Device

μPD43256BCZ: 28-pin plastic DIP (600 mil)

| Soldering process | Soldering conditions |
|-----------------------------------|---|
| Wave soldering (only to leads) | Solder temperature: 260 °C or below, Flow time: 10 seconds or below |
| Partial heating method | Terminal temperature: 300 °C or below, Time: 3 seconds or below (Per one lead) |

Caution Do not jet molten solder on the surface of package.

[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

[MEMO]

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NEC devices are classified into the following three quality grades:

"Standard", "Special", and "Specific". The Specific quality grade applies only to devices developed based on a customer designated "quality assurance program" for a specific application. The recommended applications of a device depend on its quality grade, as indicated below. Customers must check the quality grade of each device before using it in a particular application.

Standard: Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment and industrial robots

Special: Transportation equipment (automobiles, trains, ships, etc.), traffic control systems, anti-disaster systems, anti-crime systems, safety equipment and medical equipment (not specifically designed for life support)

Specific: Aircrafts, aerospace equipment, submersible repeaters, nuclear reactor control systems, life support systems or medical equipment for life support, etc.

The quality grade of NEC devices is "Standard" unless otherwise specified in NEC's Data Sheets or Data Books. If customers intend to use NEC devices for applications other than those specified for Standard quality grade, they should contact an NEC sales representative in advance.

Anti-radioactive design is not implemented in this product.