How to Use the DMA CRC Generator on PIC32MX/ PIC32MZ/PIC32MM Devices

Introduction

The Cyclic Redundancy Check (CRC) is a robust error-checking algorithm to ensure the integrity of data before it is processed. The CRC value (checksum) is associated with a message or a particular block of data. Whether it is a data packet for communication or a block of data stored in memory, CRC helps to validate it before processing.

The CRC calculation is an iterative process and it consumes considerable CPU bandwidth when implemented in software. The CRC block in the Special Function Module (SFM) integrated in the DMA module on PIC32MX/PIC32MZ/PIC32MM devices facilitates a fast and efficient CRC checksum calculation with minimal software overhead.

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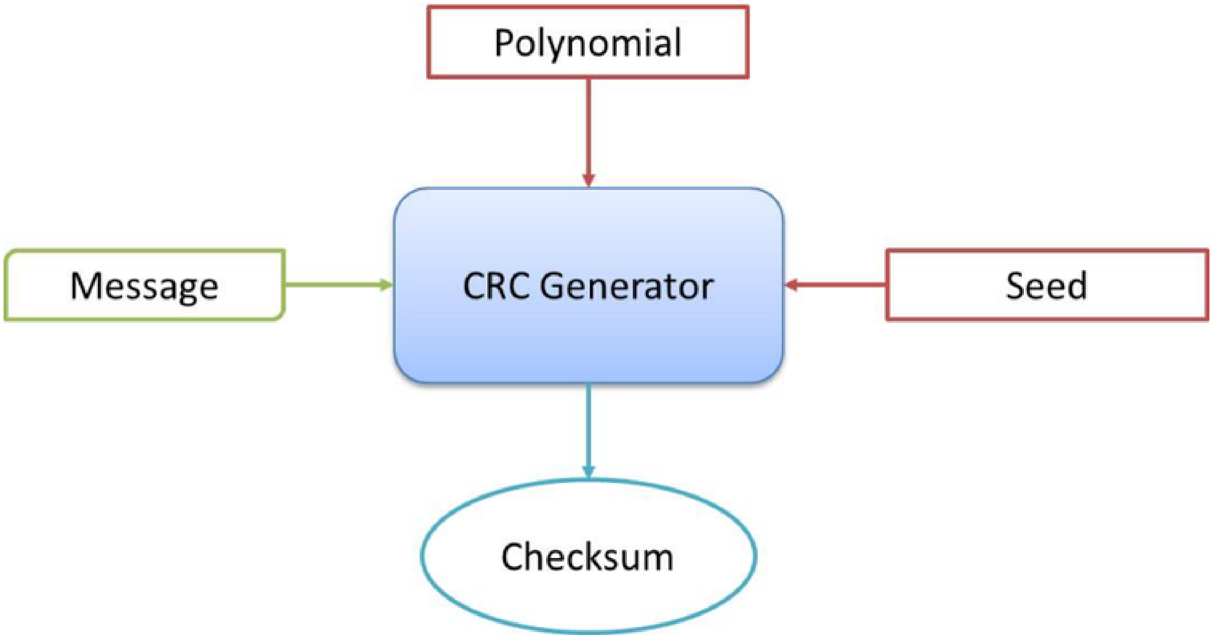
1. Concept

The block diagram of a CRC generator engine is shown in the following figure.

Figure 1-1. CRC Generator



Polynomial

The CRC calculation is an iterative process of performing the XOR operation. The CRC algorithm uses a *Polynomial* to perform its calculations. The divisor, dividend and remainder that are represented by numbers are termed as *polynomials with binary coefficients*.

For example, the number, 19h (11001b), is represented in the following equation:

(1*x4) + (1*x3) + (0*x2) + (0*x1) + (1*x0) or **x4 + x3 + x0**

The application uses a suitable generator polynomial to detect errors using CRC. Some widely used polynomials are given in the following table.

Table 1-1. Polynomial Functions for Common CRC

Name	Hex Value	Polynomial
CRC-16	0x8005	$x^{16} + x^{15} + x^{2} + 1$
CRC-CCITT	0x1021	$x^{16} + x^{12} + x^{5} + 1$
CRC-XMODEM	0x8408	$x^{16} + x^{15} + x^{10} + x^{3}$
CRC-32	0x04C11DB7	$x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^{8} + x^{7} + x^{5} + x^{4} + x^{2} + x^{1} + 1$

Seed

The seed is the desired initial value for the CRC used by the algorithm to start the computation. The seed can be a direct or non-direct value. The direct seed algorithm does not require the *n*-zero bits to be appended at the end of the message for computing the *n*-bit CRC. The non-direct seed algorithm requires the *n* zero bits to be appended at the end of the message for computing the *n*-bit CRC. 16-zero bits need to be appended to the message for a 16-it CRC computation, and 32-zero bits need to be appended to the message for a 32-bit CRC computation.

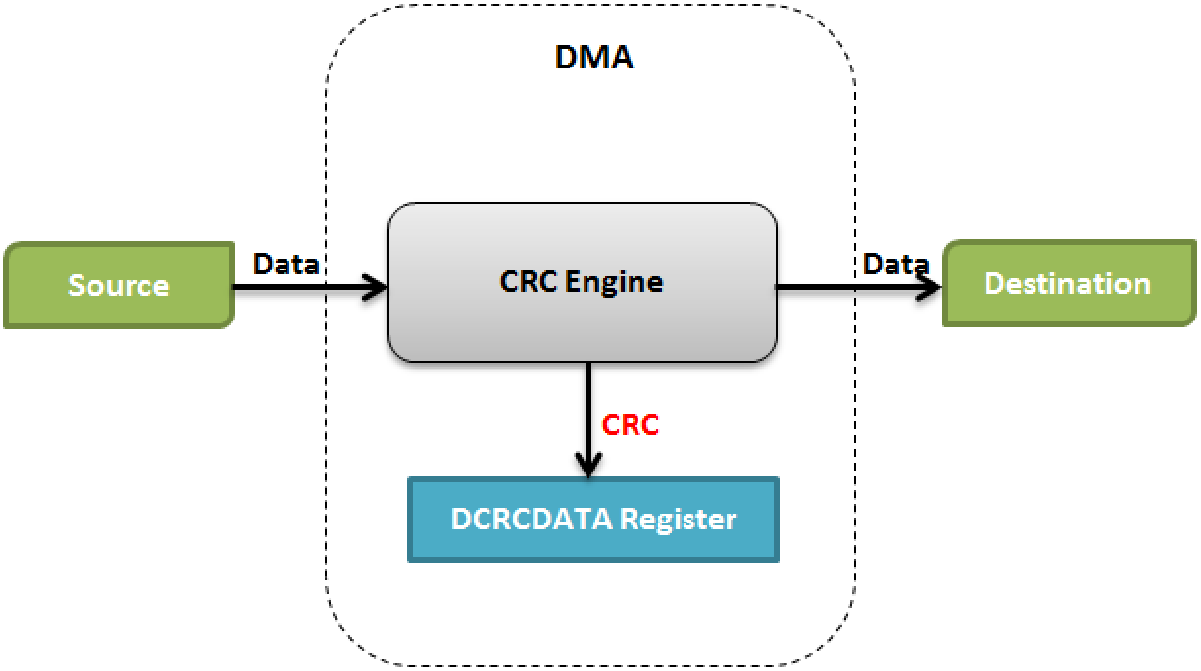
Non-direct seeds can be obtained by the XOR direct seed. The computed CRC is same for the direct or non-direct seeded algorithms. The choice of initial seed being a direct or non-direct value is decided based on the ability of the CRC algorithm to avoid the augmented zeros at the end of the message.

Note: The DMA module on PIC32MX/PIC32MZ/PIC32MM devices has a SFM. The SFM has a Linear Feedback Shift Register (LFSR) CRC engine. The LFSR CRC engine attached to DMA allows parallel CRC computation as data transfers from source to destination over DMA channels. The DMA CRC engine is compatible to direct and non-direct seeded CRC computations. The DMA CRC engine has two modes of operation, Background mode and Append mode.

Background Mode

The CRC engine attached to the DMA on PIC32MX/PIC32MZ/PIC32MM devices has a Background mode. In this mode, the DMA channel associated for CRC computation maintains its default behavior. The DMA reads the data from the source, passes it through the CRC module, and writes it to the destination as shown in the following figure.

Figure 1-2. Background Mode CRC

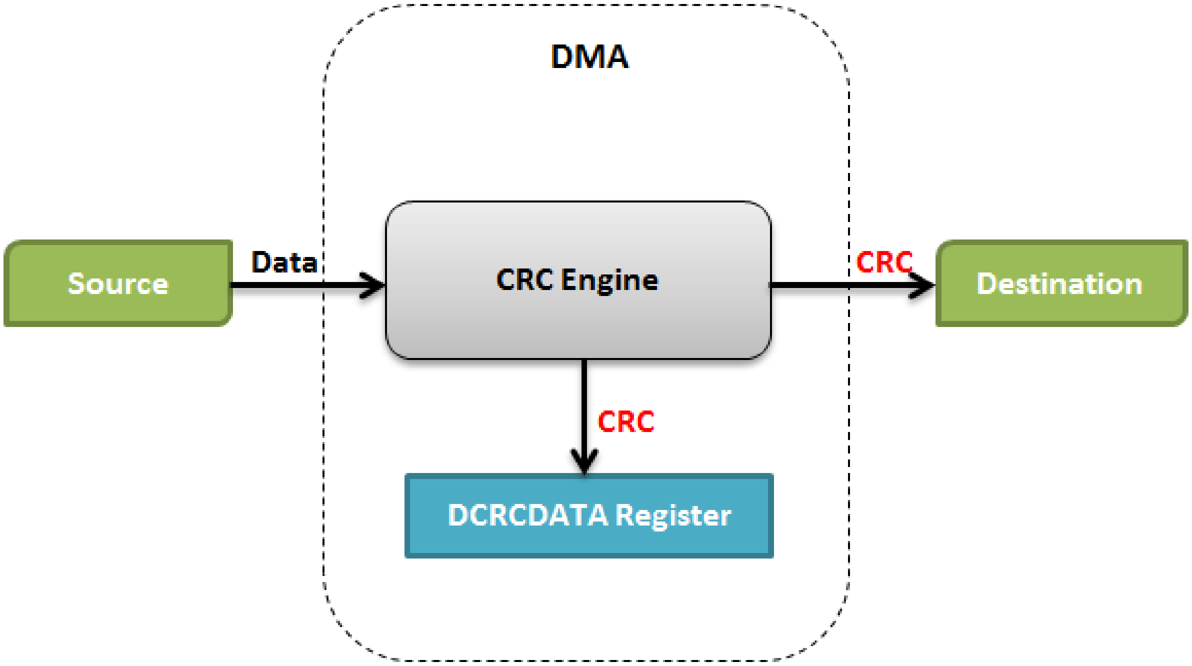


When the data transmission is completed, the calculated CRC is available in the DCRCDATA register.

Append Mode

The CRC engine attached to the DMA on PIC32MX/PIC32MZ/PIC32MM devices has an Append mode. In this mode, the DMA channel associated for CRC computation only feeds the data from the source to the CRC engine. It does not write the data to the destination, instead when a data transmission completes, it writes the computed CRC to the destination and the DCRCDATA register as shown in the following figure.

Figure 1-3. Append Mode CRC



2. Solution

The DMA system service under Microchip's MPLAB Harmony software framework provides the support to implement CRC computation. The following is the sequence of steps used in an MPLAB Harmony-based project to compute the CRC of data using the CRC engine tied to the DMA peripheral.

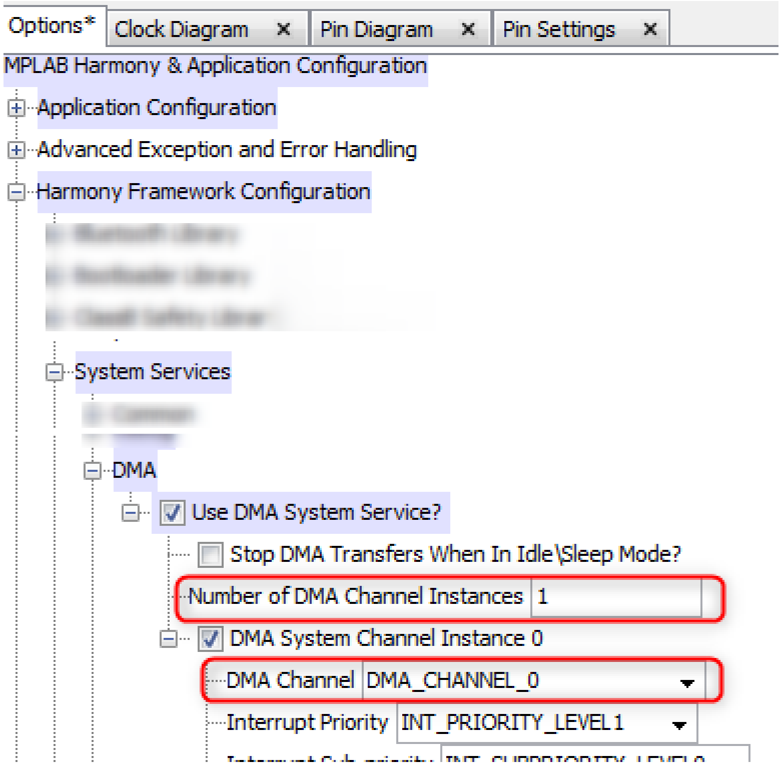
1. Configure a DMA channel using MHC.
2. Open the DMA channel.
3. Register DMA channel event handler.
4. Setup DMA operation characteristics.
5. Setup the CRC computation.
6. Setup and initiate data transfer.
7. Observe the CRC result.

Configure DMA Channel using MHC:

The DMA channel used for CRC computation is configured using the MHC (MPLAB Harmony Configurator) tool as shown in the following figure.

Expand the *MPLAB Harmony Configurator* > *Options* > *System Services* > *DMA* selection tree.

Figure 2-1. DMA Channel Configuration

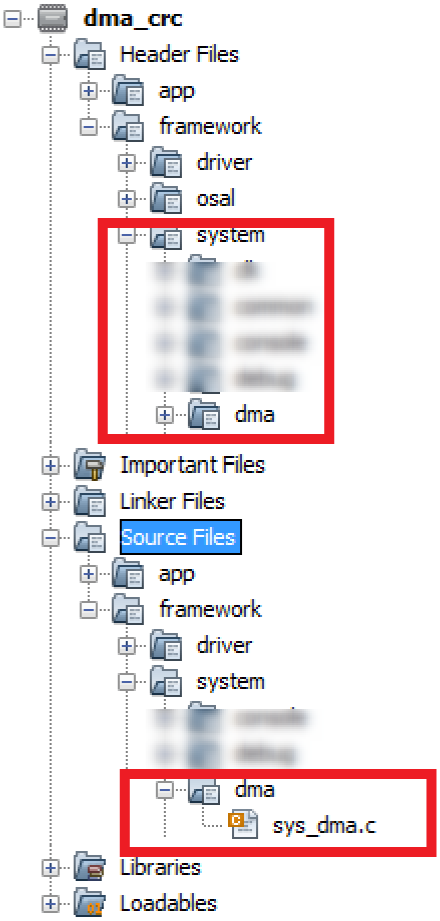


MPLAB Harmony & Application Configuration
- Application Configuration
- Advanced Exception and Error Handling
- Harmony Framework Configuration
  - System Services
    - DMA
      - ☑ Use DMA System Service?
        - □ Stop DMA Transfers When In Idle\Sleep Mode?
        - Number of DMA Channel Instances: 1
        - ☑ DMA System Channel Instance 0
          - DMA Channel: DMA_CHANNEL_0
          - Interrupt Priority: INT_PRIORITY_LEVEL1
          - Interrupt Sub-priority: INT_SUBPRIORITY_LEVEL0

Note:

1. The configured DMA channel could be associated with a Harmony driver (USART, SPI, and so on) if the data transfer is to/from the peripheral associated with the Harmony driver.
2. The configuration shown previously adds the DMA system service library to your Harmony project. The folder structure shown in the following figure is added to the project when you generate the code with the above DMA channel configuration.

Figure 2-2. DMA System Service Folders

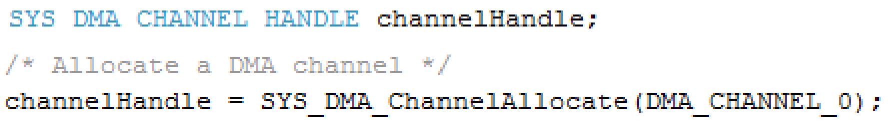


3. The generated code initializes the configured DMA channel by calling the function *SYS_DMA_Initialize* in file `system_init.c`.

Open the DMA Channel:

In the application code, get a handle to the configured DMA channel by calling the DMA system service function *SYS_DMA_ChannelAllocate*, as shown in the following figure.

Figure 2-3.



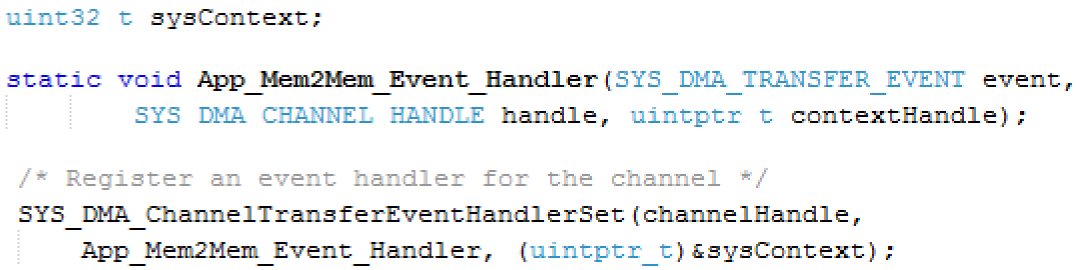
```
SYS_DMA_CHANNEL_HANDLE channelHandle;

/* Allocate a DMA channel */
channelHandle = SYS_DMA_ChannelAllocate(DMA_CHANNEL_0);
```

Note: If the configured DMA channel is associated with a Harmony driver (USART, SPI, and so on), the application need not call the function *SYS_DMA_ChannelAllocate* explicitly as the channel will have been allocated by the driver.

Register DMA channel Event Handler:

In the application code, register an even handler for the opened DMA channel by calling the DMA system service function *SYS_DMA_ChannelTransferEventhandlerSet* as shown in the following figure.

Figure 2-4.



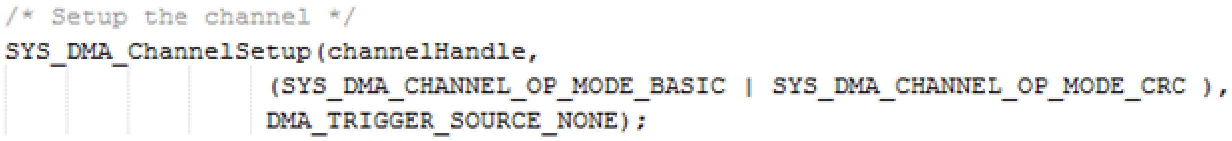
```
uint32_t sysContext;

static void App_Mem2Mem_Event_Handler(SYS_DMA_TRANSFER_EVENT event,
            SYS_DMA_CHANNEL_HANDLE handle, uintptr_t contextHandle);

 /* Register an event handler for the channel */
 SYS_DMA_ChannelTransferEventHandlerSet(channelHandle,
     App_Mem2Mem_Event_Handler, (uintptr_t)&sysContext);
```

Note: If the configured DMA channel is associated with a Harmony driver (USART, SPI, and so on) the application need not call the function *SYS_DMA_ChannelTransferEventhandlerSet* explicitly as the event handler for the channel is registered by the driver.

Setup DMA operation characteristics:

In the application code, setup (operation mode and channel trigger source) the registered DMA channel for CRC enabled operation by calling the DMA system service function *SYS_DMA_ChannelSetup* as shown in the following figure.

Figure 2-5.



```
/* Setup the channel */
SYS_DMA_ChannelSetup(channelHandle,
                    (SYS_DMA_CHANNEL_OP_MODE_BASIC | SYS_DMA_CHANNEL_OP_MODE_CRC ),
                    DMA_TRIGGER_SOURCE_NONE);
```

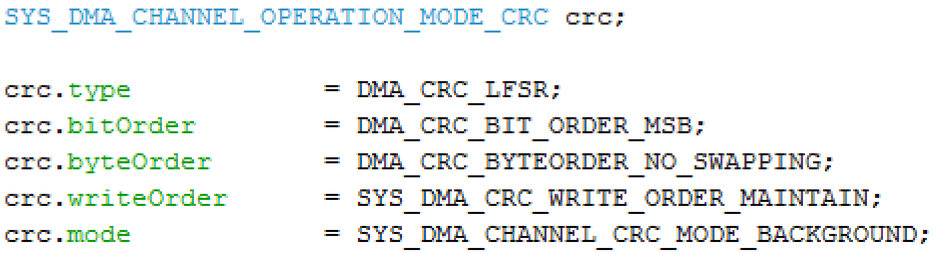
Note: If the configured DMA channel is associated with a Harmony driver (USART, SPI, and so on), enable the CRC operation by calling the DMA Harmony PLIB function *PLIB_DMA_CRCEnable* as shown in the following code.

```
PLIB_DMA_CRCENABLE ( DMA_ID_0) ;
```

Setup the CRC Computation:

The *crc* structure fields, *type*, *bitOrder*, *byteOrder* and *writeOrder* are set according to the desired values as shown in the following figure.

Figure 2-6.



```
SYS_DMA_CHANNEL_OPERATION_MODE_CRC crc;

crc.type          = DMA_CRC_LFSR;
crc.bitOrder      = DMA_CRC_BIT_ORDER_MSB;
crc.byteOrder     = DMA_CRC_BYTEORDER_NO_SWAPPING;
crc.writeOrder    = SYS_DMA_CRC_WRITE_ORDER_MAINTAIN;
crc.mode          = SYS_DMA_CHANNEL_CRC_MODE_BACKGROUND;
```

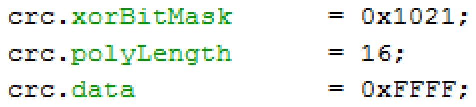
Note:

1. The field mode is set to *SYS_DMA_CHANNEL_CRC_MODE_BACKGROUND* when Background mode is desired.
2. The field mode is set to *SYS_DMA_CHANNEL_CRC_MODE_APPEND* when Append mode is desired.

The fields *xorBitMask* (polynomial value), *polyLength* (polynomial length in bits) and *data* (initial seed value) are inputs to the CRC engine.

To compute the CRC for a 16-bit CRC-CCIT polynomial (0x1021) with an initial seed of 0xFFFF, the structure of the *crc* fields are set as shown in the following figure.

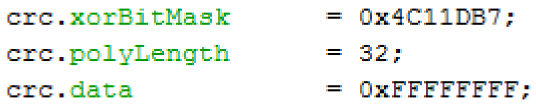
Figure 2-7.



```
crc.xorBitMask      = 0x1021;
crc.polyLength      = 16;
crc.data            = 0xFFFF;
```

To compute the CRC for a 32-bit CRC-32 polynomial (0x4C11DB7) with an initial seed of 0xFFFFFFFF, the structure of the *crc* fields are set as shown in the following figure.

Figure 2-8.



```
crc.xorBitMask      = 0x4C11DB7;
crc.polyLength      = 32;
crc.data            = 0xFFFFFFFF;
```

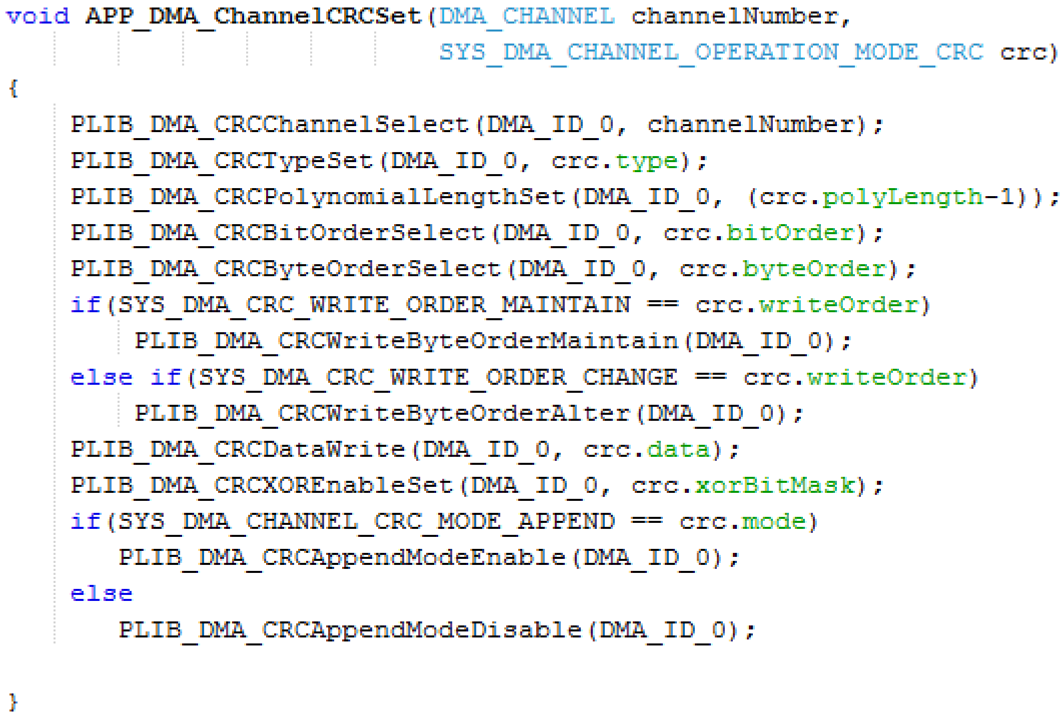
In the application code, setup the CRC computation for the DMA channel setup for the CRC enabled operation by calling the DMA system service function *SYS_DMA_ChannelCRCSet* as shown in the following code.

```
SYS_DMA_ChannelCRCSet (channelHandle, crc) ;
```

Note:

1. If the configured DMA channel is associated with a Harmony driver (USART, SPI, and so on), implement the following function (by using the DMA PLIB functions) to setup the CRC computation for the configured DMA channel.

   Figure 2-9.

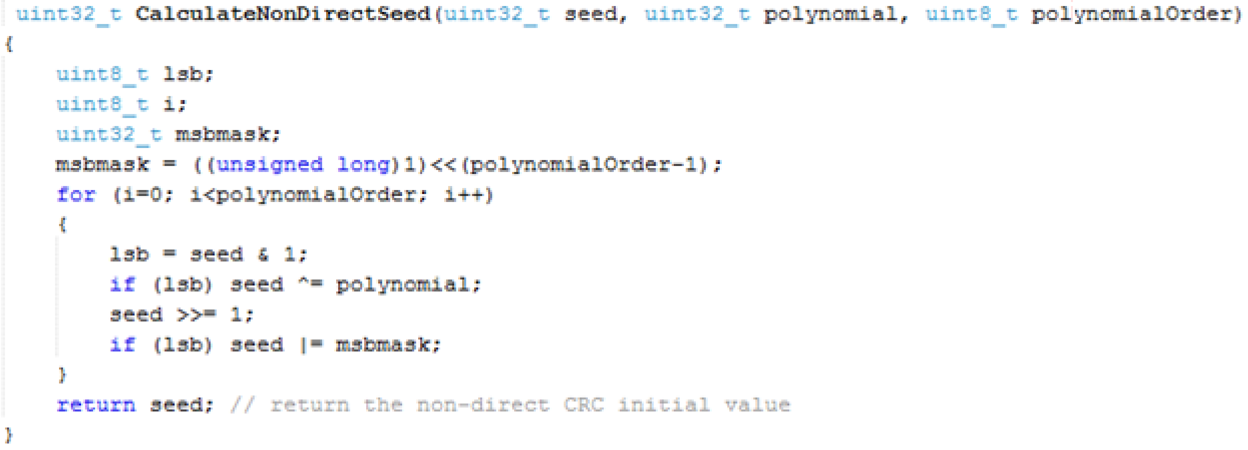
```
void APP_DMA_ChannelCRCSet(DMA_CHANNEL channelNumber,
                           SYS_DMA_CHANNEL_OPERATION_MODE_CRC crc)
{
    PLIB_DMA_CRCChannelSelect(DMA_ID_0, channelNumber);
    PLIB_DMA_CRCTypeSet(DMA_ID_0, crc.type);
    PLIB_DMA_CRCPolynomialLengthSet(DMA_ID_0, (crc.polyLength-1));
    PLIB_DMA_CRCBitOrderSelect(DMA_ID_0, crc.bitOrder);
    PLIB_DMA_CRCByteOrderSelect(DMA_ID_0, crc.byteOrder);
    if(SYS_DMA_CRC_WRITE_ORDER_MAINTAIN == crc.writeOrder)
        PLIB_DMA_CRCWriteByteOrderMaintain(DMA_ID_0);
    else if(SYS_DMA_CRC_WRITE_ORDER_CHANGE == crc.writeOrder)
        PLIB_DMA_CRCWriteByteOrderAlter(DMA_ID_0);
    PLIB_DMA_CRCDataWrite(DMA_ID_0, crc.data);
    PLIB_DMA_CRCXOREnableSet(DMA_ID_0, crc.xorBitMask);
    if(SYS_DMA_CHANNEL_CRC_MODE_APPEND == crc.mode)
       PLIB_DMA_CRCAppendModeEnable(DMA_ID_0);
    else
       PLIB_DMA_CRCAppendModeDisable(DMA_ID_0);

}
```

2. Setup the CRC computation for the configured DMA channel by calling the function *APP_DMA_ChannelCRCSet* as shown in the following code.

```
APP_DMA_ChannelCRCSet (DMA_CHANNEL_0, crc) ;
```

For comparing results, if a non-direct seed is required to be used for CRC computation, convert and use the direct seed to non-direct seed as shown in the following figure.

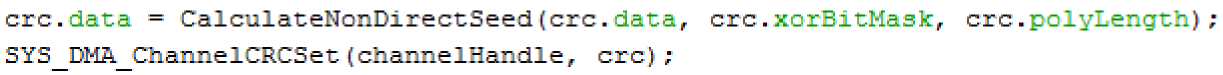
Figure 2-10.



```
uint32_t CalculateNonDirectSeed(uint32_t seed, uint32_t polynomial, uint8_t polynomialOrder)
{
    uint8_t lsb;
    uint8_t i;
    uint32_t msbmask;
    msbmask = ((unsigned long)1)<<(polynomialOrder-1);
    for (i=0; i<polynomialOrder; i++)
    {
        lsb = seed & 1;
        if (lsb) seed ^= polynomial;
        seed >>= 1;
        if (lsb) seed |= msbmask;
    }
    return seed; // return the non-direct CRC initial value
}
```

Before calling the function *SYS_DMA_ChannelCRCSet or APP_DMA_ChannelCRCSet,* convert the direct seed to non-direct by calling the function *CalculateNonDirectSeed* as shown in the following figure.

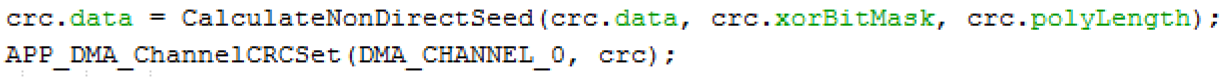
Figure 2-11.



```
crc.data = CalculateNonDirectSeed(crc.data, crc.xorBitMask, crc.polyLength);
SYS_DMA_ChannelCRCSet(channelHandle, crc);
```

Or

Figure 2-12.



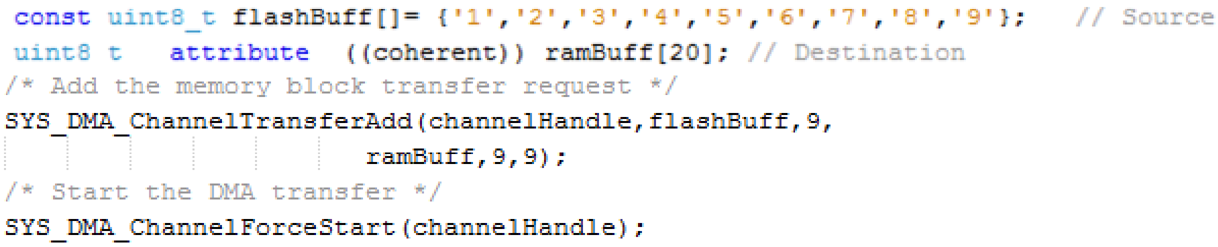
```
crc.data = CalculateNonDirectSeed(crc.data, crc.xorBitMask, crc.polyLength);
APP_DMA_ChannelCRCSet(DMA_CHANNEL_0, crc);
```

Setup and Initiate Data transfer:

Data transfer between memory to memory

Call the *SYS_DMA_ChannelTransferAdd* function to setup the data transfer, and initiate the data transfer by calling the function *SYS_DMA_ChannelForceStart*. To transfer 9 bytes of ASCII data “123456789” from Flash memory to RAM while computing the CRC as shown in the following figure.

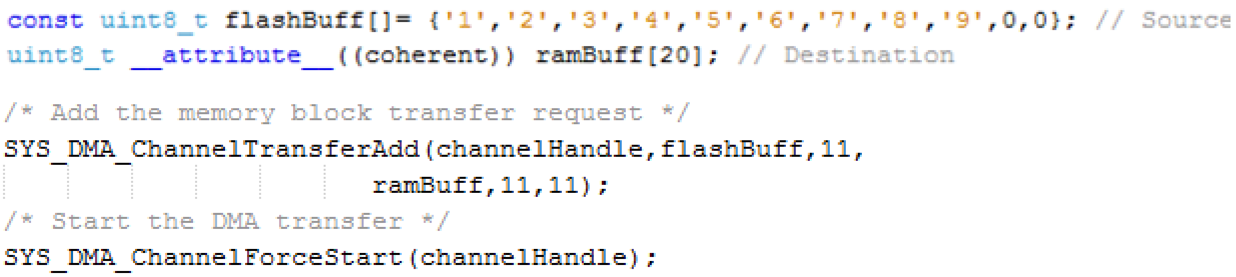
Figure 2-13.



```
const uint8_t flashBuff[]= {'1','2','3','4','5','6','7','8','9'};   // Source
uint8 t   attribute   ((coherent)) ramBuff[20]; // Destination
/* Add the memory block transfer request */
SYS_DMA_ChannelTransferAdd(channelHandle,flashBuff,9,
                           ramBuff,9,9);
/* Start the DMA transfer */
SYS_DMA_ChannelForceStart(channelHandle);
```

Note: If a non-direct seed is applied during the CRC computation (as explained in section ***Setup the CRC Computation*** above), append additional zero bits (16-bit or 32-bit, depending on the polynomial length) as shown in the following figure.

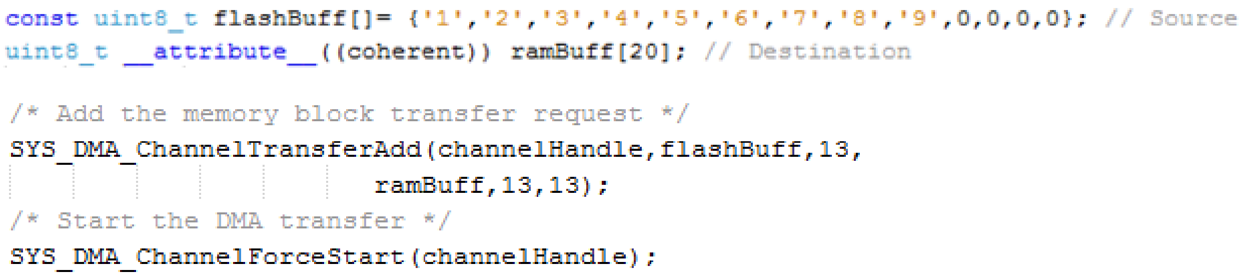
Figure 2-14. For a 16-bit Polynomial



```
const uint8_t flashBuff[]= {'1','2','3','4','5','6','7','8','9',0,0}; // Source
uint8_t __attribute__((coherent)) ramBuff[20]; // Destination

/* Add the memory block transfer request */
SYS_DMA_ChannelTransferAdd(channelHandle,flashBuff,11,
                                ramBuff,11,11);
/* Start the DMA transfer */
SYS_DMA_ChannelForceStart(channelHandle);
```

- The arguments source *(srcAddr)* and destination *(destAddr) to function call SYS_DMA_ChannelTransferAdd* needs to append 2 bytes of zeros (corresponding to the polynomial length).
- The arguments source size (*srcSize*), destination size(*destSize*) and cell size(*cellSize*) *to function call SYS_DMA_ChannelTransferAdd* needs to add value 2 (depending to the polynomial length).

Figure 2-15. For 32-bit Polynomial



```
const uint8_t flashBuff[]= {'1','2','3','4','5','6','7','8','9',0,0,0,0}; // Source
uint8_t __attribute__((coherent)) ramBuff[20]; // Destination

/* Add the memory block transfer request */
SYS_DMA_ChannelTransferAdd(channelHandle,flashBuff,13,
                                ramBuff,13,13);
/* Start the DMA transfer */
SYS_DMA_ChannelForceStart(channelHandle);
```

- The arguments source *(srcAddr)* and destination *(destAddr) to function call SYS_DMA_ChannelTransferAdd* needs to append 4 bytes of zeros (Corresponding to the polynomial length)
- The arguments source size (*srcSize*), destination size(*destSize*) and cell size(*cellSize*) *to function call SYS_DMA_ChannelTransferAdd* needs to add value 4 (depending to the polynomial length)

Data transfer between memory and a peripheral

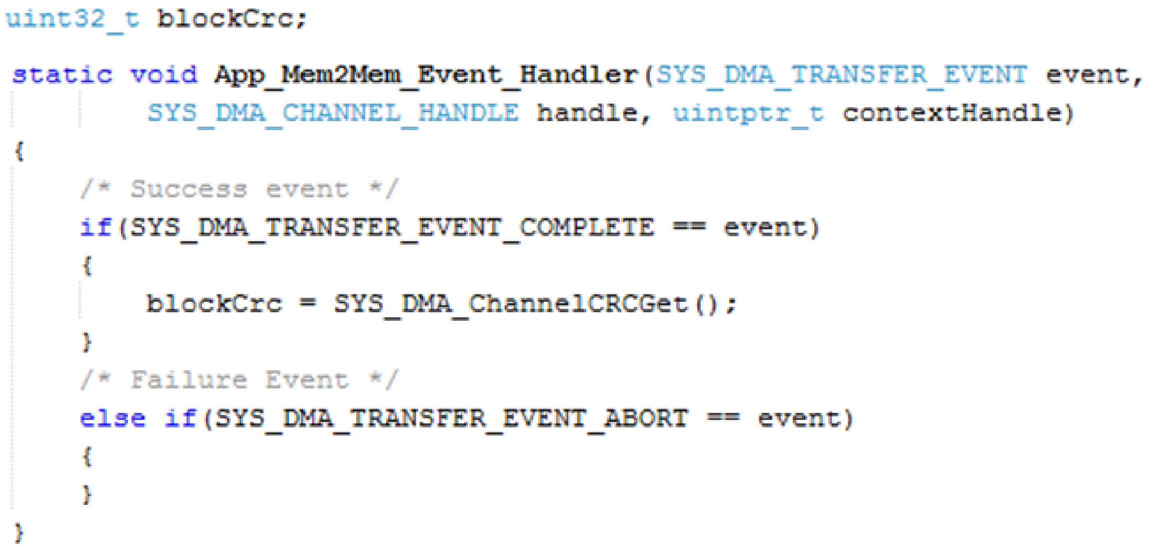
Call the peripheral driver function that sets up and enables the data transfer. If data is transferred from memory to the USART (for transmission) using the DMA in a buffered data model, the function *DRV_USART_BufferAddWrite needs to be called.*

Note: If a non-direct seed is applied during the CRC computation (as explained in section ***Setup the CRC Computation*** above), append additional zeros (2 or 4, depending on polynomial length) for the argument source (*buffer*), and add value (2 or 4, depending on polynomial length) for the argument size (*size*).

Observe the CRC computation result:

- If the data is transferred between memory-to-memory, on data transfer completion, the event handler is registered using the function *SYS_DMA_ChannelTransferEventhandlerSet would be called.* In the event handler, call the function *SYS_DMA_ChannelCRCGet* and observe the generated CRC.

Figure 2-16.



```
uint32_t blockCrc;

static void App_Mem2Mem_Event_Handler(SYS_DMA_TRANSFER_EVENT event,
        SYS_DMA_CHANNEL_HANDLE handle, uintptr_t contextHandle)
{
    /* Success event */
    if(SYS_DMA_TRANSFER_EVENT_COMPLETE == event)
    {
        blockCrc = SYS_DMA_ChannelCRCGet();
    }
    /* Failure Event */
    else if(SYS_DMA_TRANSFER_EVENT_ABORT == event)
    {
    }
}
```

- If the data transfer is between the memory and a peripheral, on data transfer completion, the event handler registered using the peripheral driver *would be called.* In the driver event handler, call the function *SYS_DMA_ChannelCRCGet* and observe the generated CRC.

3. Relevant Resources

For additional information, refer to these docs which are available for download form the following locations:

Cyclic Redundancy Check (CRC)

- http://ww1.microchip.com/downloads/en/AppNotes/01148a.pdf

CRC Generating and Checking

- http://ww1.microchip.com/downloads/en/AppNotes/00730a.pdf

32-Bit Programmable Cyclic Redundancy Check (CRC)

- http://ww1.microchip.com/downloads/en/DeviceDoc/60001336c.pdf

Cyclic Redundancy Code (CRC) Polynomial Selection For Embedded Networks

- http://users.ece.cmu.edu/~koopman/roses/dsn04/koopman04_crc_poly_embedded.pdf

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PART NO.	[X][(1)]	–X	/XX
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	E	= -40°C to +125°C (Extended)
Package:	AA	= Package AA
	BB	= Package BB

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- MCPXXXXXBT-E/BB: Tape and Reel Extended temperature, XBB package

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