

Module Name: Transceiver nRF24L01+ Module with Chip Antenna

1) Pin Description:

- A. **GND** : Connects to System Ground
- B. **IRQ** : Maskable interrupt pin. Active Low
- C. **MISO** : SPI Slave Data Output
- D. **MOSI** : SPI Slave Data Input
- E. **SCK** : SPI Clock Input
- F. **CSN** : SPI Chip Select
- G. **CE** : Chip Enable Activates RX or TX mode. CE = 0 makes the chip to go into Stand-by
- H. **VCC** : Connects to Power Supply. Input to Voltage Regulator(3V).

2) Device Features

A. Operational Modes

- i. Power down → nRF24L01+ is disabled for minimal current consumption. All register values are maintained and SPI are kept active. Entered by resetting the bit CONFIG.PWR_UP
- ii. Standby Mode
 - 1. Standby-I Mode →Minimizes average current consumption with short start up time. Entered by setting CONFIG.PWR_UP bit. Setting CE leaves the standby mode and enters active mode. When CE = LOW, the device returns to standby from TX or RX modes.
 - 2. Standby-II Mode → When CE = HIGH and TX FIFO is empty
- iii. RX mode(receiver mode)
 - 1. Entering Condition : PWR_UP bit = 1, PRIM_RX bit = 1, CE pin = 1
 - 2. If valid packet is found(matching address + valid CRC) the packet is presented in a vacant slot of RX FIFO. If FIFO are full, received packet is ignored.
 - 3. Internal Received Power Detector signal goes HIGH when RF signal higher than -64dbM is detected inside the receiving frequency channel.
- iv. TX mode(transmit mode)
 - 1. Entering Condition : PWR_UP bit = 1, PRIM_RX bit = 0, CE pin = 1(for more than 10us), Plus not empty TX FIFO
 - 2. The chip stays in TX mode until it finishes transmitting a packet as long as CE is held high. If TX FIFO is empty, the chip goes into standby-II mode.
 - 3. Never keep the chip in TX mode for more than 4ms at a time.
 - 4. Will empty all levels in TX FIFO's
 - 5. Giving CE a short pulse of 10us allows one packet to be transmitted.
- v. Air data rate
 - 1. Set in RF_SETUP.RF_DR bit
 - 2. Transmitter and the receiver should be programmed with same air data rate
 - 3. Can be 250kbps, 1Mbps, or 2Mbps.
 - 4. Lower data rate = better sensitivity, Higher data rate= lower average current
- vi. RF channel Frequency
 - 1. Set by RF_CH register according to following formular
$$F_0 = 2400 + RF_CH[\text{Mhz}]$$
 - 2. Can operate on frequencies from 2.400GHz to 2.525GHz.
 - 3. Programming resolution of channel frequency is 1Mhz.
 - 4. Bandwidth_{250Kbps, 1Mbps} = 1Mhz, Bandwidth_{2Mbps} = 2Mhz

- vii. Received Power Detection
 1. RPD bit is located in register 09 bit 0
 2. $RPD = 1$ if $Power_{received} > -64\text{dbm}$, and $RPD = 0$ if $Power_{received} < -64\text{dbm}$.
 3. Can be read any time when the chip is in RX mode

- viii. Power Amplifier control
 1. Sets the output power from the chip's power amplifier
 2. Controlled by RF_PWR bits in the RF_SETUP register.
 3. $RF_PWR = 11$

RF_PWR	RF output power
11	0dBm
10	-6dBm
01	-12dBm
00	-18dBm

- ix. RX/TX control
 1. Controlled by PRIM_RX bit in CONFIG register.

B. Enhanced ShockBurst™ (Automatic packet handling and timing)

- i. Looks at address and CRC for valid reception.
- ii. When the chip receives valid payload, it is moved into a vacant slot in the FIFOs
- iii. Packet transaction starts by Primary Transmitter(PTX) transmitting a packet. The transaction is complete when the Primary Receiver(PRX) sends
- iv. Automatic packet transaction process.
 1. PTX sends a data packet from PTX to PRX. The chip automatically sets the PTX in receive mode to wait for ACK packet.
 2. If packet is received by PRX, the chip on the receiver side transmits ACK packet to the PTX before returning to receive mode.
 3. If PTX does not get ACK packet immediately, the chip on the transmitter automatically resends the original packet after delay(programmable)
 4. Maximum number of retransmits and delay for next retransmission is configurable.
 5. The user of the data chip do not have to worry about automatic packet transaction process

v. Packet Format

Preamble(1 byte)	Address (3-5 byte)	Packet Control Field 9 bit	Payload 0-32byte	CRC 1-2 byte
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1. Preamble : Used by PRX to sync with incoming bit streaming
 - A. Either 10101010 or 01010101. Depending on the first bit of the Address field, the first bit of the preamble is automatically set to 0 or 1 to provide smooth transition between the Preamble and the Address field(do not allow 11 or 00 in the transition)
2. Address
 - A. Assures that the packet is detected and received by the correct receiver.
3. Packet Control field

Payload length 6bit	PID 2bit	NO_ACK 1bit
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- A. Payload Length
 - i. This field is only used if Dynamic Payload Length function is enabled

- ii. 000000 = 0 byte. 100000 = 32 byte, 100001 = Don't car
- B. PID(Packet identification)
- i. Used to determine if the received packet is new or retransmitted.
 - ii. Prevents the PRX device from presenting the same payload more than once to host MCU.
 - iii. PID is incremented each time new packet is received by TX side through SPI. Thus, if the receiving side sees same PID value in a row, it looks at CRC to determine if it has received the duplicate packet.
- C. No_ACK
- i. NO_ACK = 1 tells the receiver that the packet is not to be auto acknowledged.
 - ii. You can set NO_ACK flag with command, W_TX_PAYLOAD_NOACK after enabling the function by setting the EN_DYN_ACK in FEATURE register.
 - iii. When you use this option PTX goes directly to standby-I mode after transmitting the packet.
- D. Payload
- i. The chip provides two options for handling payload length: static and dynamic
 1. Static (Default option)→fixed packet length
 - A. Set by RX_PW_px registers on the receiver side
 - B. Transmitter should make sure that the number of bytes clocked into the TX_FIFO is equal to that that set aside by the receiver side.
 2. Dynamic payload length→ Variable packet length
 - A. Enable EN_DPL bit in the FEATURE register to use DPL. DYNPD register must be set. The PTX must have DPL_P0 bit in DYNPD set.
 - B. The chip automatically decodes the length of decoded packet(does not use RX_PW_Px registers).
 - C. MCU can read the length of the received payload by using the R_RX_PL_WID command.
 - D. Always check that the packet width is shorter or equal to 32 when using R_RX_PL command. If it is longer than 32 bytes, the packet contains error and should be discarded by using Flush_RX command.
- E. CRC(Error checking code)
- i. The number of bytes in CRC is set by CRCO bit in the CONFIG register.
 - ii. If CRC fails no packet is received.
4. Automatic Packet transaction handling
- A. Auto acknowledgment
- i. Enabled by setting the EN_AA register.
 - ii. PRX device automatically sends ACK packet to the PTX when it receives valid packet.
 - iii. If the received packet has NO_ACK flag set, auto acknowledgement is not executed.
 - iv. An ACK packet can contain an optional payload from PRX to PTX.
 1. Enabled by setting EN_ACK_PAY in the feature register.
 2. DPL must be enabled
 3. The MCU on the PRX side has to upload the payload by clocking it into the TX FIFO by using W_ACK_PAYLOAD command.

4. The pay load is pending in TX FIFO(PRX) until new packet is received from the PTX.
 5. Can have three ACK packet payloads pending in the TX FIFO(PRX) at the same time.
 - 6.
 - v. MCU can flush the TX FIFO by using the FLUSH_TX command
- B. Auto Retransmission(TX side)
- i. Maximum number of retry can be setup by ARC bits in the SETUP_RETR register.
 - ii. Retransmits a packet if a ACK packet is not received.
 - iii. PTX enters RX mode and waits for a short period for an ACK packet each time a packet is transmitted
 - iv. If the ACK packet is not received, the chip goes back to TX mode after the delay defined by ARD(auto retransmission delay) and retransmits the data.
 1. ARD is set up in SETUP_RETR register in steps of 250us.
 2. ARD must never be shorter than the sum of the startup time and the time on-air(basically a time required for the receiver to send data)
 3. ARD = 500us is long enough for any ACK payload length in 2 or 1Mbps mode
 4. For 250kbps, look at the table in the device data sheet.
 - v. Two packet loss counters are incremented each time a packet is lost.
 1. ARC_CNT counts the number of retransmissions for the current transaction.
 2. ARC_CNT is reset by initiating a new transaction.
 3. PLOS_CNT counts the total number of retransmission since the last channel change.
 4. PLOS_CNT is reset by writing to the RF_CH register.
 5. Used to measure the channel quality.
 - vi. As an alternative, you can manually set the number of times for the packet to be retransmitted.
 - vii. IF ACK packet contains a payload, both TX_DS IRQ and RX_DR IRQ are asserted before the chip returns to standby-I mode.
 - viii. For state flowchart, for PRX and PTX information, look at the datasheet 7.5.1 and 7.5.2
 - ix. A copy of previously received packet might be received if the ACK packet is lost. In this case, the PRX discards the received packet and transmits an ACK packet before it returns to RX mode.
- C. Multiceiver
- i. PRX may have a set of six parallel data pipes with unique addresses.
 - ii. Each data pipe has its own physical address(data pipe address)
 - iii. Can receive data addressed to six different data pipes in *one frequency channel*.
 - iv. Thus, Up to six nRF24L01+s configured as PTX can communicate with one nRF24L01+ configured as PRX.
 - v. Only one data pipe can receive a packet at a time.
 - vi. 5 byte data address with 4 most significant bytes are shared among pipes and the least significant bytes distinguish each data pipes.
 - vii. When transmitting ACK packet, the PRX uses the data pipe's address to make sure that the

correct PTX receives the ACK signal.

- D. Transaction IRQs
 - i. RX_DR IRQ is asserted after the packet is received by PRX.
 - ii. TX_DS IRQ is asserted when the packet is acknowledged and the ACK packet is received by the PTX.
 - iii. MAX_RT IRQ is asserted if the auto retransmit counter(ARC_CNT) exceeds the programmed maximum limit(ARC). The payload in TX FIFO is NOT removed, and the MCU decides the next step in the protocol. The payload can be removed from the TX FIFO using the FLUSH_TX command.
- 3) Data and Control Interface(SPI)
 - A. Every new command must be started by a high to low transition on CSN
 - B. STATUS register is serially shifted out on the MISO pin simultaneously to the SPI Command word shifting in to the MOSI pin
 - C. Serial shifting SPI commands
 - i. <Command word: MSBit to LSBit(one byte)>
 - 1. For list of command word, look at page 51 of the datasheet.
 - ii. <Data bytes : LSByte to MSByte, MSBit in each byte first>
 - D. TX FIFO in a PRX is blocked if all pending payloads are addressed to pipes where the link to PTX is lost. In this case, the MCU can flush TX FIFO using the FLUSH_TX command
 - E. RX FIFO in PRX can contain payloads from up to three different PTX devices and TX FIFO in PTX can have up to three payloads stored.
- 4) Interrupt(IRQ pin)
 - A. Active Low
 - B. Activated when TX_DS, RX_DR, or MAX_RT IRQ are set high.
 - C. IRQ pin is reset when MCU writes '1' to the IRQ source bit in the STATUS register.
 - D. IRQ mask in the CONFIG register is used to select the IRQ sources that are allowed to assert the IRQ pin. Setting one of the MASK bits high disables the corresponding IRQ.
 - E. By default all IRQ sources are enabled.
- 5) Register Map.
 - A. Look in the datasheet pg.57 for the list of registers and their addresses.
 - B. Pay careful attention to the reset value.
 - C. You configure the radio by accessing the register map through the SPI.
- 6) MultiCeiver
 - A. LSByte must be unique for all six pipes.