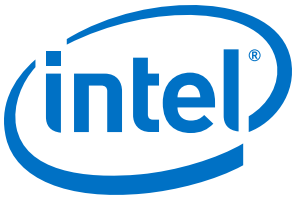

PowerPlay Early Power Estimator User Guide

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Contents

1 PowerPlay Early Power Estimator Overview

This user guide describes the PowerPlay Early Power Estimator (EPE) support for Arria® II, Arria V, Cyclone® III, Cyclone IV, Cyclone V, Stratix® III, Stratix IV, Stratix V, and MAX® 10 device families. This user guide provides guidelines to use the PowerPlay EPE at any stage of the FPGA design and provides details about thermal analysis and the factors that contribute to FPGA power consumption. You can calculate the FPGA power with the Microsoft Excel-based PowerPlay EPE spreadsheet. For more accurate power estimation, use the PowerPlay Power Analyzer in the Quartus® II or Quartus Prime software.

Intel recommends switching from the PowerPlay EPE spreadsheet to the PowerPlay Power Analyzer in the Quartus II or Quartus Prime software once the design is available. The PowerPlay Power Analyzer has access to the implemented design details to produce more accurate results.

Intel recommends using these calculations as an estimation of power, not as a specification. You must verify the actual power during device operation as the information is sensitive to the actual device design and the environmental operating conditions.

The features of the PowerPlay EPE spreadsheet include:

- Estimating the power consumption of your design before creating the design or during the design process
- Importing device resource information from the Quartus II or Quartus Prime software into the PowerPlay EPE spreadsheet with the use of the Quartus II or Quartus Prime-generated PowerPlay EPE file
- Performing preliminary thermal analysis of your design

Related Links

- PowerPlay Power Analysis chapter in volume 3 of the Quartus II Handbook
- PowerPlay Early Power Estimator for Intel CPLDs User Guide

1.1 Release Information

Release information describes the supported device families and version of the PowerPlay EPE spreadsheet, which is documented in this user guide.

You should always use the latest version of the PowerPlay EPE spreadsheet.

Related Links

PowerPlay Early Power Estimators (EPE) and Power Analyzer

1.2 Power Model Status for Supported Device Families

The power models in the PowerPlay EPE spreadsheet are either in preliminary or final status. Preliminary power models are subject to change. Preliminary power models are created based on simulation results, process data, and other known parameters. The final power models are created based on a complete correlation to the production device. If the power models are final, there are no further changes to the power models. The power model status for the device will be shown in the Main worksheet of the PowerPlay EPE spreadsheet.

For the majority of the designs, the PowerPlay Power Analyzer and the PowerPlay EPE spreadsheet have the following accuracy after the power models are final:

- PowerPlay Power Analyzer: ± 20% from silicon, assuming that PowerPlay Power Analyzer uses the Value Change Dump File (`.vcd`) generated toggle rates
- PowerPlay EPE spreadsheet: ± 30% from silicon, assuming PowerPlay EPE data imported from PowerPlay Power Analyzer results using `.vcd` generated toggle rates

The toggle rates are derived using the PowerPlay Power Analyzer with a `.vcd` file generated from a gate level simulation representative of the system operation.

Related Links

PowerPlay Early Power Estimators (EPE) and Power Analyzer

2 Setting Up the PowerPlay Early Power Estimator

2.1 System Requirements

The PowerPlay EPE spreadsheet requires the following software:

- Windows operating system that the Quartus II software supports
- Microsoft Excel 2003, Microsoft Excel 2007, or Microsoft Excel 2010
- Quartus II software version 9.1 or later (if generating a file for import)

Related Links

Operating System Support

2.2 Download and Install the PowerPlay Early Power Estimator

The PowerPlay EPE spreadsheet for Intel devices is available from the *PowerPlay Early Power Estimators (EPE)* and Power Analyzer on www.altera.com. After reading the terms and conditions and clicking **I Agree**, you can download the Microsoft Excel (`.xls` or `.xlsx`) file.

By default, the macro security level in Microsoft Excel 2003, Microsoft Excel 2007, and Microsoft Excel 2010 is set to **High**. If the macro security level is set to **High**, macros are automatically disabled. For the features in the PowerPlay EPE spreadsheet to function properly, you must enable macros.

2.2.1 Changing the Macro Security Level in Microsoft Excel 2003

To change the macro security level in Microsoft Excel 2003, follow these steps:

1. Click **Tools ➤ Options**.
2. Click **Security ➤ Macro Security**.
3. Select **Security Level ➤ Medium** in the **Security** dialog box then click **Ok**.
4. Click **Ok** in the **Options** window.
5. Close the PowerPlay EPE spreadsheet and reopen it.
6. Click **Enable Macros** in the pop-up window.

2.2.2 Changing the Macro Security Level in Microsoft Excel 2007

To change the macro security level in Microsoft Excel 2007, follow these steps:

1. Click the **Office** button in the upper left corner of the `.xlsx` file.
2. Click the **Excel Options** button at the bottom of the menu.
3. Click the **Trust Center** button on the left. Then, click the **Trust Center Settings** button.
4. Click the **Macro Settings** button in the **Trust Center** dialog box. Turn on the **Disable all macros with notification** option.
5. Close the PowerPlay EPE spreadsheet and reopen it.
6. Click **Options** when a security warning appears beneath the Office ribbon.
7. Turn on **Enable this content** in the **Microsoft Office Security Options** dialog box.

2.2.3 Changing the Macro Security Level in Microsoft Excel 2010

To change the macro security level in Microsoft Excel 2010, follow these steps:

1. Click **File**
2. Click **Help ➤ Options**
3. Click **Trust Center ➤ Trust Center Settings**
4. Click the **Macro Settings** button in the **Trust Center** dialog box. Turn on the **Disable all macros with notification** option.
5. Close the PowerPlay EPE spreadsheet and reopen it.
6. Click **Enable Content** when a security warning appears beneath the Office ribbon.

2.3 Estimating Power Consumption

You can use the PowerPlay EPE spreadsheet to estimate the power consumption at any point of your design cycle. You can use the PowerPlay EPE spreadsheet to estimate the power consumption if you have not begun your design, or if your design is not complete. While the PowerPlay EPE spreadsheet can provide you with an estimate for your complete design, Intel strongly recommends using the PowerPlay Power Analyzer in the Quartus II or Quartus Prime software for precise information of the exact placement and routing information of the design.

2.3.1 Estimating Power Consumption Before Starting the FPGA Design

Table 1. Advantage and Constraints of Power Estimation before Designing FPGA

Advantage	Constraint
You can obtain power estimation before starting your FPGA design.	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • The PowerPlay EPE spreadsheet uses averages and not the actual design implementation details; for example ALUT input usage and routing. The PowerPlay Power Analyzer has access to the full design details.

To estimate power consumption with the PowerPlay EPE spreadsheet before starting your FPGA design, follow these steps:

1. On the Main worksheet of the PowerPlay EPE spreadsheet, select the target family, device, and package from the **Family**, **Device**, and **Package** drop-down list.
2. Enter values for each worksheet in the PowerPlay EPE spreadsheet. Different worksheets in the PowerPlay EPE spreadsheet display different power sections, such as clocks and phase-locked loops (PLLs).
3. The calculator displays the total estimated power consumption in the `Total FPGA` and `Total SoC` (if applicable) cells of the Main worksheet.

2.3.1.1 Entering Information into the PowerPlay Early Power Estimator

You can either manually enter power information into the PowerPlay EPE spreadsheet or load a PowerPlay EPE file generated by the Quartus II software. You can also clear all current values in the PowerPlay EPE spreadsheet by clicking the **Reset** button on the Main worksheet.

To use the PowerPlay EPE spreadsheet, enter the device resources, operating frequency, toggle rates, and other parameters in the PowerPlay EPE spreadsheet. If you do not have an existing design, you must estimate the number of device resources your design uses and enter the information into the PowerPlay EPE spreadsheet.

Related Links

Estimating Power Consumption Before Starting the FPGA Design on page 6

2.3.1.1.1 Manually Entering Values

You can manually enter values into the PowerPlay EPE spreadsheet in the appropriate section. White unshaded cells are input cells that you can modify. Each section contains a column that allows you to specify a module name based on your design.

2.3.2 Estimating Power Consumption While Creating the FPGA Design

If your FPGA design is partially complete, you can import the PowerPlay EPE file (<*revision name*>`_early_pwr.csv`) generated by the Quartus II software to the PowerPlay EPE spreadsheet. After importing the information from the <*revision name*>`_early_pwr.csv` into the PowerPlay EPE spreadsheet, you can edit the PowerPlay EPE spreadsheet to reflect the device resource estimates for your final design.

Table 2. Advantages and Constraints of Power Estimation if your FPGA Design is Partially Complete

Advantage	Constraint
• You can perform power estimation early in the FPGA design cycle. • Provides the flexibility to automatically fill in the PowerPlay Early Power Estimator spreadsheet based on the Quartus II software compilation results.	• Accuracy depends on your inputs and your estimation of the device resources; where this information may change (during or after your design is complete), your power estimation results may be less accurate. • The PowerPlay EPE spreadsheet uses averages and not the actual design implementation details; for example ALUT input usage and routing. The PowerPlay Power Analyzer has access to the full design details.

2.3.2.1 Importing a File

To estimate power consumption with the PowerPlay EPE spreadsheet if your FPGA design is partially complete, you can import a file.

Importing a file saves you time and effort otherwise spent on manually entering information into the PowerPlay EPE. You can also manually change any of the values after importing a file.

2.3.2.1.1 Generate the PowerPlay EPE File

To generate the PowerPlay EPE file, follow these steps:

1. Compile the partial FPGA design in the Quartus II software.
2. On the Project menu, click **Generate PowerPlay Early Power Estimator File** to generate the <*revision name*>_early_pwr.csv in the Quartus II software.

2.3.2.1.2 Import Data into the PowerPlay EPE Spreadsheet

You must import the PowerPlay EPE file into the PowerPlay EPE spreadsheet before modifying any information in the PowerPlay EPE spreadsheet. Also, you must verify all your information after importing a file.

Importing a file from the Quartus II software populates all input values on the Main worksheet that were specified in the Quartus II software. These parameters include:

- Family
- Device
- Package
- Temperature grade
- Power characteristics
- Core voltage (V)
- Ambient (T_A) or junction (T_J) temperature (°C)
- Heat sink
- Airflow
- Custom θ_{SA} or Custom θ_{JA}
- Board thermal model

The ambient or junction temperature, heat sink, airflow, Custom θ_{SA} or Custom θ_{JA}, and board thermal model parameters are optional. For more information about these parameters, refer to the Main worksheet.

The clock frequency (f_{MAX}) values imported into the PowerPlay EPE spreadsheet are the same as the f_{MAX} values taken from the Quartus II software as per the design. You can manually edit the f_{MAX} values and the toggle percentage in the PowerPlay EPE spreadsheet to suit your design requirements.

To import data into the PowerPlay EPE spreadsheet, follow these steps:

1. In the PowerPlay EPE spreadsheet, Click **Import CSV**.
2. Browse to a PowerPlay EPE file generated from the Quartus II software and click **Open**. The file has a name of <*revision name*>_early_pwr.csv.
3. In the confirmation window to proceed, click **OK**.
4. If the file is imported, click **OK**. Clicking **OK** acknowledges the import is complete. If there are any errors during the import, an `.err` file is generated with details.

Related Links

Main Worksheet on page 10

2.3.3 Estimating Power Consumption After Completing the FPGA Design

If your design is complete, Intel strongly recommends using the PowerPlay Power Analyzer in the Quartus II software. The PowerPlay Power Analyzer provides the most accurate estimate of device power consumption. To determine power consumption, the PowerPlay Power Analyzer uses simulation, user mode, and default toggle rate assignments, in addition to placement-and-routing information.

Related Links

PowerPlay Power Analysis chapter in volume 3 of the Quartus II Handbook

3 PowerPlay Early Power Estimator Worksheets

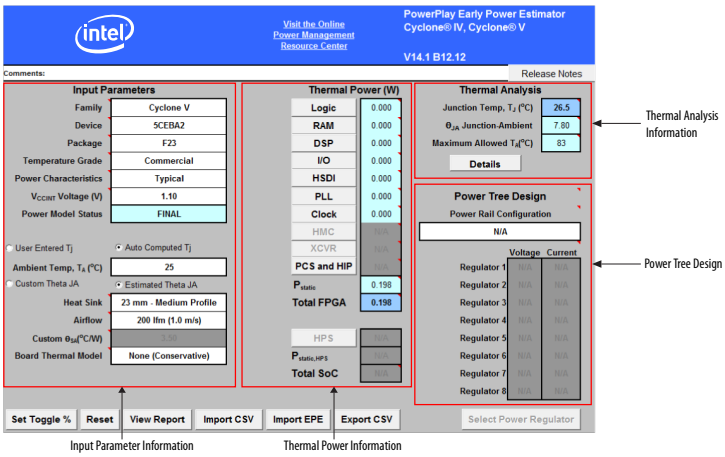
This chapter provides information about each worksheet of the PowerPlay EPE spreadsheet. The PowerPlay EPE spreadsheet provides the ability to enter information into worksheets based on architectural features. The PowerPlay EPE spreadsheet also provides a subtotal of power consumed by each architectural feature and is reported in each worksheet in watts. For more information about each architectural feature refer to the respective worksheets.

Related Links

3.1 Main Worksheet

The Main worksheet of the PowerPlay EPE spreadsheet summarizes the power and current estimates for the design. The Main worksheet displays the total thermal power, thermal analysis, and power supply sizing information.

Figure 1. Main Worksheet of the PowerPlay EPE Spreadsheet



For EPE 14.0 onwards, **Export CSV** feature was added to provide a lightweight export file as compared to the EPE file. The generated `.csv` file has a similar file format to the EPE spreadsheet. The following sections describe the sections in the Main worksheet of the PowerPlay EPE spreadsheets.

3.1.1 Input Parameter

The required parameters depend on whether the junction temperature is manually entered or auto computed.

Table 3. Input Parameter Section Information

Input Parameter	Description
Family	Select the device family.
Device	Select your device. Larger devices consume more static power and have higher clock dynamic power. All other power components are unaffected by the device used.
Package	Select the package that is used. Larger packages provide a larger cooling surface and more contact points to the circuit board, leading to lower thermal resistance. Package selection does not affect dynamic power.
Temperature Grade	Select the appropriate temperature grade. This field affects the allowed maximum junction temperature range. This field can also be used to determine core voltage for some device families. Different device families support different temperature grades. For more information about the supported temperature grade and the recommended operating range for the device junction temperature, refer to the respective device family datasheet.
Power Characteristic	Select typical or theoretical worst-case silicon process. There is a process variation from die-to-die. This primarily impacts the static power consumption. **Typical** power characteristic provides results that line up with average device measurements. **Maximum** power characteristic provides results that line up with worst-case device measurements. To ensure your power supply design is sufficient to handle the worst-case process variation that affects static power

continued...

Input Parameter	Description
	consumption, Intel recommends using the **Maximum** power characteristic for your power estimation. To enable the Enpirion device selection, you must set Power Characteristics to **Maximum**.
V_{CCINT} Voltage (V)	For Cyclone IV E devices, select the following V_{CCINT} voltage: • For devices with speed grade C8L, C9L and I8L, set the V_{CCINT} to **1.0V**. • For devices with speed grade C6, C7, C8, I7 and A7, set the VCCINT to **1.2V**.
V_{CC_ONE} Voltage (V)	For MAX 10 devices only, select 3.0 V or 3.3 V. The voltage is internally regulated to 1.2 V to supply power to the core and periphery.
Power Model Status	This shows if the power model for the device is in preliminary or final version and is only available from EPE 14.0 onwards.
V_{CCL} Voltage (V)	For Stratix III devices, select the following V_{CCL} voltage: • For devices with speed grade –4L, this value can either be **0.9 V** or **1.1 V**. • For devices with other speed grades, set the VCCL voltage level to **1.1 V**.
Junction Temp, T_J (°C)	Enter the junction temperature of the device. This field is only available if you turn on the **User Entered T** option. In this case, the junction temperature is not calculated based on the thermal information provided. For Enpirion power device selection, Intel recommends setting **Junction Temp, T (°C)** to the highest value for the chosen temperature grade.
Ambient Temp, T_A (°C)	Enter the air temperature near the device. This value can range from **–40°C** to **125°C**. This field is only available when you turn on the **Auto Computed T** option. If you turn on the **Estimated Theta J** option, this field is used to compute the junction temperature based on power dissipation and thermal resistance through the top-side cooling solution (heat sink or none) and board (if applicable). If you turn on the **Custom Theta J** option, this field is used to compute junction temperature based on power dissipation and custom θ_{JA} entered.
Heat Sink	Select the heat sink that is used. You can select one of the following: • No heat sink (**None**) • A custom solution (**Custom**) • A heat sink with set parameters (**15 mm–Low Profile**, **23 mm–Medium Profile**, or **28 mm–High Profile**). This field is only available if you turn on the **Auto Computed T** and **Estimated Theta J** options. If you select **None**, the heat sink selection updates the custom θ_{SA} value and you can see the value in the Custom θ_{SA} (°C/W) parameter. If you select **Custom**, the value is what is entered in the Custom θ_{SA} (°C/W) parameter. Representative examples of heat sinks are provided. Larger heat sinks provide lower thermal resistance and lower the junction temperature. If the heat sink is known, consult the heat sink datasheet and enter a custom θ_{SA} value according to the airflow in your system.
Airflow	Select an available ambient airflow in linear-feet per minute (lfm) or meters per second (m/s). The values are **100 lfm (0.5 m/s)**, **200 lfm (1.0 m/s)**, **400 lfm (2.0 m/s)**, or **Still Air**. This field is only available if you turn on the **Auto Computed T** and **Estimated Theta J** options. Increased airflow results in a lower case-to-air thermal resistance and lowers the junction temperature.
Custom θ_{JA} (°C/W)	Enter the junction-to-ambient thermal resistance between the device and ambient air (in °C/W). This field is only available if you turn on the following options:

continued...

Input Parameter	Description
	• **Auto Computed T** • **Estimated Theta J** • Set the Heat Sink parameter to **Custom** To compute the overall junction-to-ambient resistance through the top of the device, the Custom θ_{SA} parameter is combined with a representative case-to-heatsink resistance and an Intel-provided junction-to-case thermal resistance.
Board Thermal Mode	Select the type of board that is used in the thermal analysis. The value is **None (Conservative)**, **Typical Board**, or **JEDEC (2s2p)**. This field is only available if you turn on the **Auto Computed T** and **Estimated Theta J** options. If you select **None (Conservative)**, the thermal model assumes no heat is dissipated through the board, resulting in a pessimistic calculated junction temperature. This option is not available if the **Heat Sink** option is set to **None**. If you select **Typical Board**, the thermal model assumes the characteristics of a typical customer board stack, which is based on the selected device and package. If you select **JEDEC (2s2p)**, the thermal model assumes the characteristics of the JEDEC 2s2p test board specified in standard JESDEC51–9. To determine the final junction temperature, Intel recommends performing a detailed thermal simulation of your system. This two-resistor thermal model is only for early estimation.

3.1.2 Thermal Power

Thermal power is the power dissipated in the device. Total thermal power is a sum of the thermal power of all the resources used in the device, including the maximum power from standby and dynamic power.

Total thermal power only includes the thermal component for the I/O section and does not include the external power dissipation, such as from voltage-referenced termination resistors.

The static power (P_{STATIC}) is the thermal power dissipated on chip, independent of user clocks. P_{STATIC} includes the leakage power from all FPGA functional blocks, except for I/O DC bias power and transceiver DC bias power, which are accounted for in the I/O and transceiver sections.

P_{STATIC} is the only thermal power component which varies with junction temperature, selected device, and power characteristics (process).

The following figure shows the total thermal power (W) and P_{STATIC} consumed by the FPGA and hard processor system (HPS). The thermal power for each worksheet is displayed. To see how the thermal power for a worksheet was calculated, click on the button to view the selected worksheet.

Figure 2. Thermal Power Section in the Main Worksheet

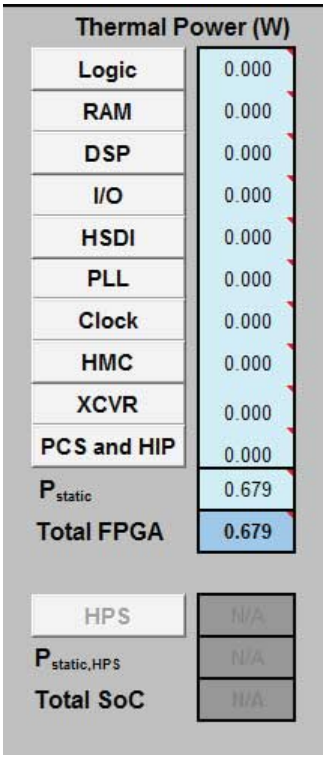


Table 4. Thermal Power Section Information

Column Heading	Description
Logic	This value shows the dynamic power consumed by adaptive logic modules (ALMs) and associated routing. To view details, click the **Logic** button.
RAM	This value shows the dynamic power consumed by RAM blocks and associated routing. To view details, click the **RAM** button.
DSP	This value shows the dynamic power consumed by digital signal processing (DSP) blocks and associated routing. To view details, click the **DSP** button.
I/O	This value shows the thermal power consumed by I/O pins and associated routing. To view details, click the **I/O** button.
HSDI	This value shows the dynamic power consumed by serializer and deserializer (SERDES) hardware for high-speed differential I/O (HSDI). To view details, click the **HSDI** button.
PLL	This value shows the dynamic power consumed by phase-locked loops (PLLs). To view details, click the **PLL** button.
Clock	This value shows the dynamic power consumed by clock networks. To view details, click the **Clock** button.
HMC	This value shows the dynamic power consumed by hard memory controller (HMC). To view details, click the **HMC** button.
XCVR	This shows the thermal power consumed by transceiver hardware. This includes the standby power consumed by transceivers. To view details, click the **XCVR** button. If the value is **N/A**, the transceiver blocks are not available on the chosen device.

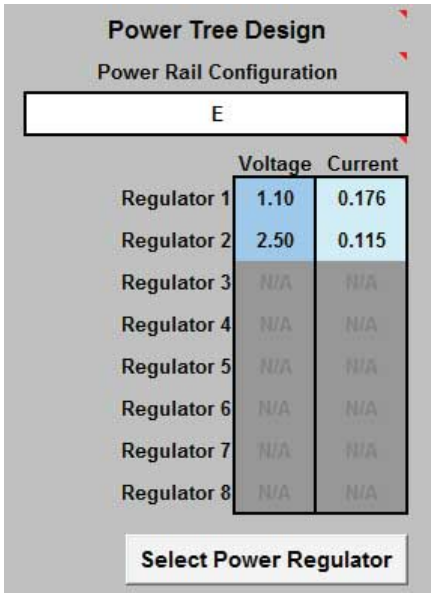
continued...

Column Heading	Description
PCS and HIP	This shows the thermal power consumed by the transceiver channel physical coding sublayer (PCS) as well as the PCI Express® (PCIe®) hard IP blocks of the transceiver hardware. This includes the standby power consumed by transceivers. To view details, click the **PCS and HIP** button. If the value is **N/A**, the transceiver blocks are not available on the chosen device.
P_{STATIC}	This shows the thermal power dissipated on chip, independent of user clocks. This includes the leakage power from all FPGA functional blocks, except for I/O DC bias power and transceiver DC bias power. P_{STATIC} is affected by junction temperature, selected device, and power characteristics. The static power for HPS is shown in $P_{STATIC,HPS}$.
Total FPGA	This shows the total power dissipated as heat from the FPGA. This does not include power dissipated in off-chip termination resistors and HPS.
HPS	This value shows the thermal power consumed by the HPS. To view the details, click the **HPS** button.
$P_{STATIC,HPS}$	This shows the thermal power dissipated from the HPS, independent of user clocks. This includes the leakage power from all HPS functional blocks, except for HPS I/O DC bias power. $P_{STATIC,HPS}$ is affected by junction temperature, selected device, and power characteristics. The static power for HPS will be turned on once the SoC device is selected.
Total SoC	This value shows the total power dissipated as heat from the FPGA and HPS. This value does not include power dissipated in off-chip termination resistors.

3.1.3 Power Tree Design

The Power Tree Design section provides the current and voltage from the report page. The power supply grouping is according to the device pin connection guidelines.

Figure 3. Power Tree Design Section in the Main Worksheet

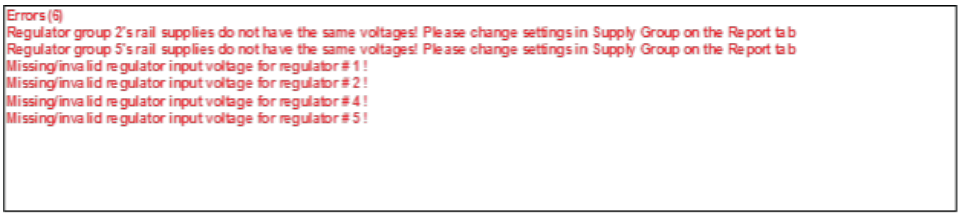


Select a valid configuration from the **Power Rail Configuration** dropdown. When the **Input Parameters** and **Power Rail Configuration** selections are complete, the power regulator selection will be enabled.

The current values shown for each regulator include the margin for regulator selection purpose. For more information, refer to the Enpirion worksheet.

Errors regarding improper rail grouping may appear in the error window on the Main worksheet when the Power Rail Configuration is selected. The following figure shows an example of the error message in the error window.

Figure 4. Error Window in the Main Worksheet



This occurs when the EPE assigns rails with different voltage requirements to the same group. Since each group is supplied by a single regulator, these errors must be corrected before the EPE can make proper component selections. This is done in the EPE Report worksheet. Refer to the Report worksheet on how to correct the error.

Related Links

- Report Worksheet on page 41
- Enpirion Worksheet on page 42

3.1.4 Thermal Analysis

The following figure shows the Thermal Analysis section in the Main worksheet, including the junction temperature (T_J), total junction-to-ambient thermal resistance (θ_{JA}), and the maximum allowed ambient temperature (T_A) values. For details about the values of the thermal parameters not listed in this user guide, click the **Details** button.

Figure 5. Thermal Analysis Section of the PowerPlay EPE Spreadsheet

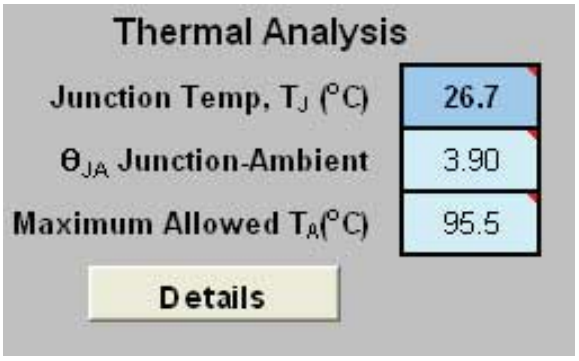


Table 5. Thermal Analysis Section Information

Column Heading	Description
Junction Temp, T_J (°C)	The device junction temperature estimation based on supplied thermal parameters.

continued...

Column Heading	Description
	The junction temperature is determined by dissipating the total thermal power through the top of the chip and through the board (if selected). For detailed calculations, click the **Details** button.
θ_{JA} Junction-Ambient	The junction-to-ambient thermal resistance between the device and ambient air (in °C/W). Represents the increase in temperature between ambient and junction for every W of additional power dissipation.
Maximum Allowed T_A (°C)	A guideline for the maximum ambient temperature (in °C) that you can subject the device to without violating the maximum junction temperature, based on the supplied cooling solution and device temperature grade.

You can directly enter or automatically compute the junction temperature based on the information provided. To enter the junction temperature, select **User Entered T** in the **Input Parameters** section. To automatically compute the junction temperature, select **Auto Computed T** in the **Input Parameters** section.

When automatically computing the junction temperature, the ambient temperature, airflow, heat sink solution, and board thermal model of the device determine the junction temperature in °C. Junction temperature is the estimated operating junction temperature based on your device and thermal conditions.

You can consider the device as a heat source and the junction temperature is the temperature of the device. While the temperature typically varies across the device, to simplify the analysis, you can assume that the temperature of the device is constant regardless of where it is measured.

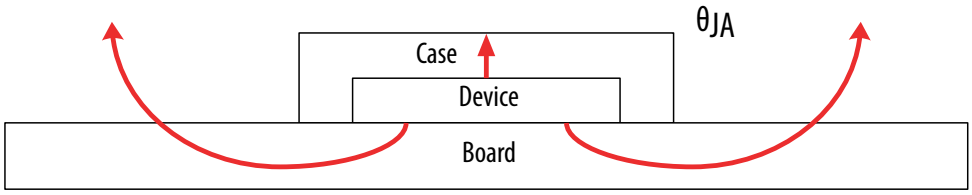
Power from the device can be dissipated through different paths. Different paths become significant depending on the thermal properties of the system. The significance of power dissipation paths vary depending on whether or not a heat sink is used for the device.

3.1.4.1 Not Using a Heat Sink

When you do not use a heat sink, the major paths of power dissipation are from the device to the air. You can refer this as a junction-to-ambient thermal resistance. In this case, there are two significant junction-to-ambient thermal resistance paths:

- From the device through the case to the air
- From the device through the board to the air

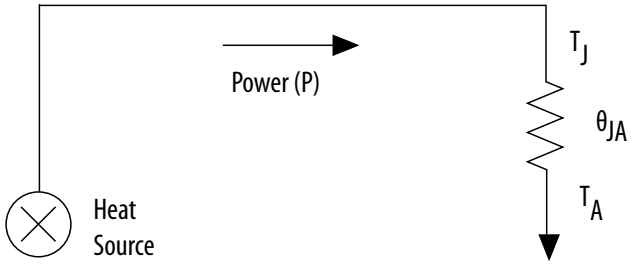
Figure 6. Thermal Representation without a Heat Sink



Thermal Representation without Heat Sink

In the model used in the PowerPlay EPE spreadsheet, power is dissipated through the case and board. The θ_{JA} values are calculated for differing air flow options accounting for the paths through the case and through the board.

Figure 7. Thermal Model in the PowerPlay EPE Spreadsheet without a Heat Sink



The ambient temperature does not change, but the junction temperature changes depending on the thermal properties; therefore the junction temperature calculation is an iterative process.

The following equation shows the total power calculated based on the total θ_{JA} value, ambient, and junction temperatures.

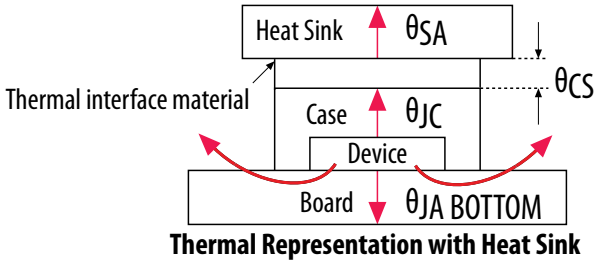
Figure 8. Total Power

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

3.1.4.2 Using a Heat Sink

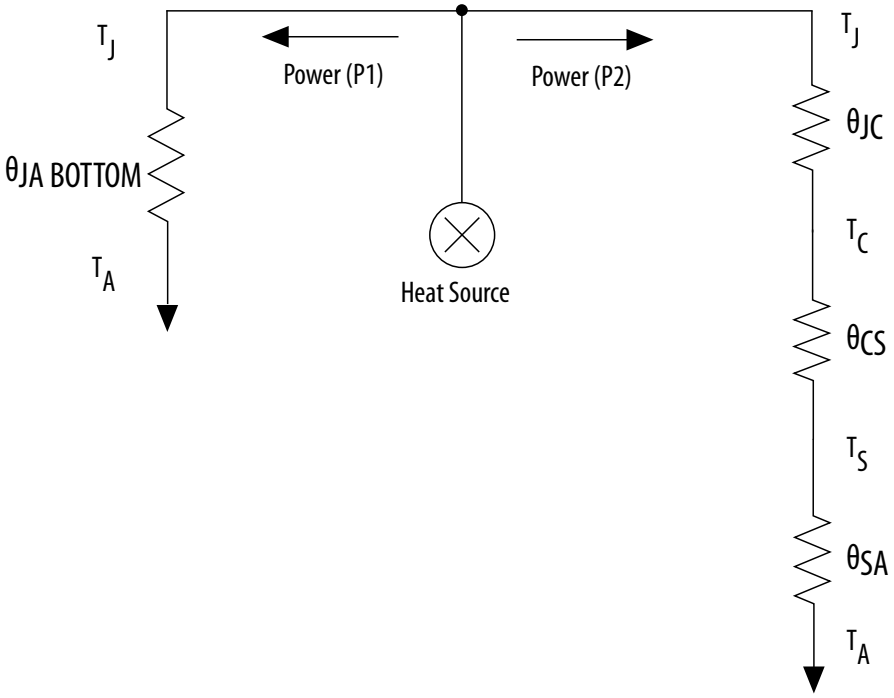
When you use a heat sink, the major paths of power dissipation are from the device through the case, thermal interface material, and heat sink. There is also a path of power dissipation through the board. The path through the board has less impact than the path to air.

Figure 9. Thermal Representation with a Heat Sink



In the model used in the PowerPlay EPE spreadsheet, power is dissipated through the board or through the case and heat sink. The junction-to-board thermal resistance ($\theta_{JA\ BOTTOM}$) refers to the thermal resistance of the path through the board. Junction-to-ambient thermal resistance ($\theta_{JA\ TOP}$) refers to the thermal resistance of the path through the case, thermal interface material, and heat sink.

Figure 10. Thermal Model for the PowerPlay EPE Spreadsheet with a Heat Sink



If you want the PowerPlay EPE spreadsheet thermal model to take the $\theta_{JA\ BOTTOM}$ into consideration, set the Board Thermal Model parameter to either **JEDEC (2s2p)** or **Typical Board**. Otherwise, set the Board Thermal Model parameter to **None (conservative)**. In this case, the path through the board is not considered for power dissipation and a more conservative thermal power estimate is obtained.

The addition of the junction-to-case thermal resistance (θ_{JC}), the case-to-heat sink thermal resistance (θ_{CS}) and the heat sink-to-ambient thermal resistance (θ_{SA}) determines the $\theta_{JA\ TOP}$.

Figure 11. Junction-to-Ambient Thermal Resistance

$$\theta_{JA\ TOP} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

Based on the device, package, airflow, and heat sink solution selected in the Input Parameters section, the PowerPlay EPE spreadsheet determines the $\theta_{JA\ TOP}$.

If you use a low, medium, or high profile heat sink, select the airflow from the values of **Still Air** and air flow rates of **100 lfm (0.5 m/s)**, **200 lfm (1.0 m/s)**, and **400 lfm (2.0 m/s)**. If you use a custom heat sink, enter the custom θ_{SA} value. You must incorporate the airflow into the custom θ_{SA} value. Therefore, the Airflow parameter is not applicable in this case. You can obtain these values from the heat sink manufacturer.

The ambient temperature does not change, but the junction temperature changes depending on the thermal properties. Because a change in junction temperature affects the thermal device properties that are used to calculate junction temperature, calculating the junction temperature is an iterative process.

The total power is calculated based on the total θ_{JA} value, ambient, and junction temperatures with the following equation.

Figure 12. Total Power

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

3.2 Logic Worksheet

Each row in the Logic worksheet of the PowerPlay EPE spreadsheet represents a separate design module. Enter the following parameters for each design module:

- Number of combinational adaptive look-up tables (ALUTs)
- Number of flipflops
- Clock frequency in MHz
- Toggle percentage
- Average fanout

Figure 13. Logic Worksheet of the PowerPlay EPE Spreadsheet

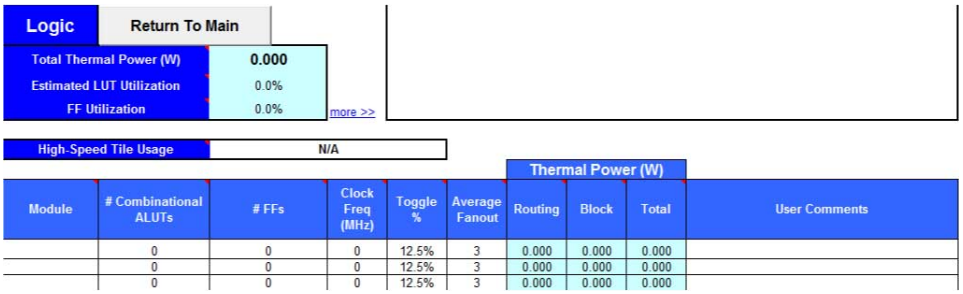


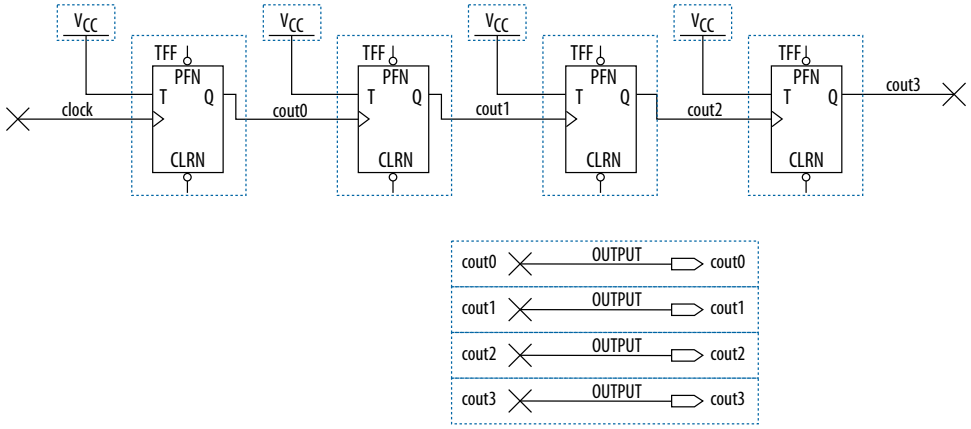
Table 6. General Settings in the Logic Worksheet

Input Parameter	Description
High-Speed Tile Usage	Select the **High-Speed Tile Usage** setting. This value can be **Typical Design**, **Typical High-Performance Design**, or **Atypical High-Performance Design**. • **Typical Design** represents a design with 10% or more timing margin. • **Typical High-Performance Design** represents an average design with no timing margin. These designs have a few near-critical timing paths. • **Atypical High-Performance Design** represents a 90th percentile design with no timing margin. These designs have many near-critical timing paths. This primarily impacts static power consumption (P_{STATIC}) found in the Main worksheet of the PowerPlay EPE spreadsheet. It also has a small impact on the dynamic power consumed by the logic resources entered in the Logic worksheet of the PowerPlay EPE spreadsheet. This option is only available for Arria V GZ, Stratix III, Stratix IV, and Stratix V devices.

Table 7. Logic Worksheet Information

Column Heading	Description
Module	Specify a name for each module of the design. This is an optional entry.
#Combinational ALUTs/#LUTs	Enter the number of combinational ALUTs or look-up tables (LUTs). This is the "Combinational ALUTs" value from the Quartus II Compilation Report Resource Usage Summary section. For Arria II, Arria V GZ, Stratix III, Stratix IV, and Stratix V devices, each adaptive logic module (ALM) contains up to two combinational ALUTs. Smaller ALUTs consume less power than larger ALUTs, but the device can fit more of them. The total number of ALUTs in the design must not exceed (the number of ALMs) × two.
#FFs	Enter the number of flipflops in the module. This is the sum of "Register ALUTs" and "Dedicated logic registers" from the Quartus II Compilation Report Resource Usage Summary section. Clock routing power is calculated separately on the Clock worksheet of the PowerPlay EPE spreadsheet.
Clock Freq (MHz)	Enter a clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. 100 MHz with a 12.5% toggle means that each LUT or flipflop output toggles 12.5 million times per second (100 × 12.5%).
Toggle%	Enter the average percentage of logic toggling on each clock cycle. The toggle percentage ranges from **0** to **100%**. Typically, the toggle percentage is 12.5%, which is the toggle percentage of a 16-bit counter. To ensure you do not underestimate the toggle percentage, use a higher toggle percentage. Most logic only toggles infrequently; therefore, toggle rates of less than 50% are more realistic. For example, a T-flipflop (TFF) with its input tied to VCC has a toggle rate of 100% because its output is changing logic states on every clock cycle. Refer to the 4-Bit Counter Example.
Average Fanout	Enter the average number of blocks fed by the outputs of the LUTs and flipflops.
Thermal Power (W)–Routing	This shows the power dissipation due to estimated routing (in watts). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power based on experimentation of more than 100 designs. For detailed analysis based on your design's routing, use the Quartus II PowerPlay Analyzer.
Thermal Power (W)–Block	This shows the power dissipation due to internal toggling of the ALMs (in watts). Logic block power is a combination of the function implemented and the relative toggle rates of the various inputs. The PowerPlay EPE spreadsheet uses an estimate based on observed behavior across more than 100 real-world designs. For accurate analysis based on your design's exact synthesis, use the Quartus II PowerPlay Analyzer.
Thermal Power (W)–Total	This shows the total power dissipation (in watts). The total power dissipation is the sum of the routing and block power.
User Comments	Enter any comments. This is an optional entry.

Figure 14. 4-Bit Counter Example



The first TFF with the `cout0` LSB output has a toggle rate of 100% because the signal toggles on every clock cycle. The toggle rate for the second TFF with `cout1` output is 50% because the signal only toggles on every two clock cycles. Consequently, the toggle rate for the third TFF with `cout2` output and fourth TFF with `cout3` output are 25% and 12.5%, respectively. Therefore, the average toggle percentage for this 4-bit counter is (100 + 50 + 25 + 12.5)/4 = 46.875%.

For more information about logic block configurations of the supported device families, refer to the "Logic Array Blocks and Adaptive Logic Modules" chapter of the respective device handbook.

3.3 RAM Worksheet

Each row in the RAM worksheet of the PowerPlay EPE spreadsheet represents a design module where the RAM blocks are the same type, have the same data width, the same RAM depth (if applicable), the same RAM mode, and the same port parameters. If some or all of the RAM blocks in your design have different configurations, enter the information in different rows. For each design module, enter the type of RAM implemented, the number of RAM blocks, and the RAM block mode.

Each row in the RAM worksheet of the PowerPlay EPE spreadsheet can also represent a logical RAM module that can be physically implemented on more than one RAM block. The PowerPlay EPE spreadsheet implements each logical RAM module with the minimum number of physical RAM blocks, in the most power-efficient way possible, based on the width and depth of the logical instance entered.

You must know how your RAM is implemented by the Quartus II Compiler when you are selecting the RAM block mode. For example, if a ROM is implemented with two ports, it is considered a true dual-port memory and not a ROM. Single-port and ROM implementations only use Port A. Simple dual-port and true dual-port implementations use Port A and Port B.

Figure 15. RAM Worksheet of the PowerPlay EPE Spreadsheet

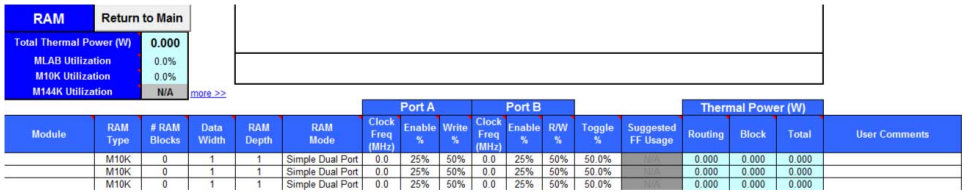


Table 8. RAM Worksheet Information

Column Heading	Description
Module	Enter a name for the RAM module in this column. This is an optional value.
RAM Type	Select the implemented RAM type. You can find the RAM type in the Type column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Click **RAM Summary**.
#RAM Blocks	Enter the number of RAM blocks in the module that use the same type and mode and have the same parameter for each port. The parameters for each port are: • Clock frequency in MHz • Percentage of time the RAM is enabled • Percentage of time the port is writing as opposed to reading You can find the number of RAM blocks in either the memory logic array block (MLAB), M9K, M10K, M20K, or M144K column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Click **RAM Summary**.
Data Width	Enter the width of the data for the RAM block. This value is limited based on the RAM type. You can find the width of the RAM block in the Port A Width or the Port B Width column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Click **RAM Summary**. For RAM blocks that have different widths for Port A and Port B, use the larger of the two widths.
RAM Depth	Enter the depth of the RAM block in number of words. You can find the depth of the RAM block in the Port A Depth or the Port B Depth column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Click **RAM Summary**.
RAM Mode	Select from the following modes: • Single-Port • Simple Dual-Port • True Dual-Port • ROM The mode is based on how the Quartus II Compiler implements the RAM. If you are unsure how your memory module is implemented, Intel recommends compiling a test case in the required configuration in the Quartus II software. You can find the RAM mode in the Mode column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Click **RAM Summary**. A single-port RAM has one port with a read and write control signal. A simple dual-port RAM has one read port and one write port. A true dual-port RAM has two ports, each with a read and write control signal. ROMs are read-only single-port RAMs.
Port A–Clock Freq (MHz)	Enter the average percentage of time the input clock enable for Port A is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from **0** to **100%**. The default value is **25%**. RAM power is primarily consumed when a clock event occurs. Using a clock enable signal to disable a port when no read or write operation is occurring can result in significant power savings.

continued...

Column Heading	Description
Port A–Write %	Enter the average percentage of time Port A of the RAM block is in write mode versus read mode. For simple dual-port (1R/1W) RAMs, the write Port A is inactive when not executing a write operation. For single-port and dual-port RAMs, Port A reads when it is not written to. This field is ignored for RAMs in ROM mode. This value must be a percentage number between **0** and **100%**. The default value is **50%**.
Port B–Clock Freq (MHz)	Enter the clock frequency for Port B of the RAM blocks in MHz. This value is limited by the maximum frequency specification for the RAM type and device family. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB.
Port B–Enable %	Enter the average percentage of time the input clock enable for Port B is active, regardless of the activity on the RAM data and address inputs. The enable percentage ranges from **0** to **100%**. The default value is 25%. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB. RAM power is primarily consumed when a clock event occurs. Using a clock-enable signal to disable a port when no read or write operation is occurring can result in significant power savings.
Port B–R/W %	For RAM blocks in true dual-port mode, enter the average percentage of time Port B of the RAM block is in write mode versus read mode. For RAM blocks in simple dual-port mode, enter the percentage of time Port B of the RAM block is reading. You cannot write to Port B in simple dual-port mode. Port B is ignored for RAM blocks in ROM or single-port mode or when the chosen RAM type is MLAB. This value must be a percentage number between **0** and **100%**. The default value is **50%**.
Toggle%	The average percentage for how often each block output signal changes value on each clock cycle is multiplied by the clock frequency and enables the percentage to determine the number of transitions per second. This only affects routing power. 50% corresponds to a randomly changing signal. A random signal changes states only half the time.
Suggested FF Usage	Displays the number of flipflops that you require to make the MLAB function correctly. The MLAB power in the RAM worksheet does not include the power of the flipflops. If you enter the device resources manually, add the suggested number of flipflops to the Logic worksheet using the same clock frequency. If you have imported the device resources from the PowerPlay EPE file, no action is required. This field is only valid when the chosen RAM type is MLAB.
Thermal Power (W)–Routing	This shows the power dissipation due to estimated routing (in watts). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power based on experimentation of more than 100 designs. For detailed analysis based on your design's routing, use the Quartus II PowerPlay Power Analyzer. This value is automatically calculated.
Thermal Power (W)–Block	This shows the power dissipation due to internal toggling of the RAM (in watts). For accurate analysis based on your design's exact RAM modes, use the Quartus II PowerPlay Power Analyzer. This value is automatically calculated.
Thermal Power (W)–Total	This shows the estimated power in watts, based on your inputs. It is the total power consumed by the RAM blocks and is equal to the routing power and block power. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the RAM block configurations of the supported device families, refer to the "Memory Blocks" chapter of the respective device handbook.

3.4 DSP Worksheet

Each row in the DSP section represents a DSP design module where all instances of the module have the same configuration, clock frequency, toggle percentage, and register usage. If some (or all) DSP or multiplier instances have different configurations, you must enter the information in different rows. Specify the following information for each DSP or multiplier module:

- Configuration
- Number of instances
- Clock frequency (in MHz)
- Toggle percentage of the data outputs
- Inputs and outputs that are registered or not
- Module pipelined or not

Figure 16. DSP Worksheet of the PowerPlay EPE Spreadsheet

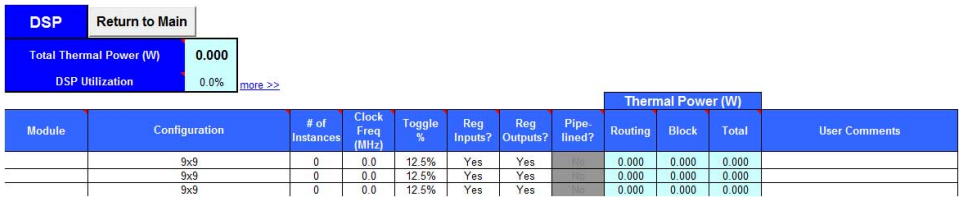


Table 9. DSP Worksheet Information

Column Heading	Description
Module	Enter a name for the DSP module in this column. This is an optional value.
Configuration	Select the DSP block configuration for the module.
# of Instances	Enter the number of DSP block instances that have the same configuration, clock frequency, toggle percentage, and register usage. This value is independent of the number of dedicated DSP blocks you use. For example, it is possible to use four 9 × 9 simple multipliers that are implemented in the same DSP block in the FPGA devices. In this case, the number of instances would be four. To determine the maximum number of instances you can fit in the device for any particular mode, follow these steps: 1. Open the "DSP Blocks", "Variable Precision DSP Blocks", or "Embedded Multipliers" chapter of the respective device handbook. 2. In the "Number of DSP Blocks" table, take the maximum number of DSP blocks available in the device for the mode of operation. 3. Divide the maximum number by the "# of Mults" for that mode of operation from the "DSP Block Operation Modes" table. 4. Use the resulting value for the "# of Instances" in the PowerPlay EPE spreadsheet.
Clock Freq (MHz)	Enter the clock frequency for the module in MHz. This value is limited by the maximum frequency specification for the device family.
Toggle %	Enter the average percentage of DSP data outputs toggling on each clock cycle. The toggle percentage ranges from **0** to **50%**. The default value is **12.5%**. For a more conservative power estimate, use a higher toggle percentage. In addition, 50% corresponds to a randomly changing signal (because half the time the signal changes from a 0-to-0 or 1-to-1). This is considered the highest meaningful toggle rate for a DSP block.

continued...

Column Heading	Description
Reg Inputs?	Select whether the inputs of the dedicated DSP block or multiplier block are registered using the dedicated input registers. If you use the dedicated input registers in the DSP or multiplier block, select **Yes**. If the inputs are unregistered or registered using registers in the ALMs or the look-up table (LUTs), select **No**.
Reg Outputs?	Select whether the outputs of the dedicated DSP block or multiplier block are registered using the dedicated input registers. If you use the dedicated output registers in the DSP or multiplier block, select **Yes**. If the inputs are unregistered or registered using registers in ALMs or LUTs, select **No**.
Pipelined?	Select whether or not the dedicated DSP block is pipelined.
Thermal Power (W)–Routing	This shows the power dissipation due to estimated routing (in watts). Routing power depends on placement and routing, which is a function of design complexity. The values shown represent the routing power based on experimentation of more than 100 designs.
Thermal Power (W)–Block	This shows the estimated power consumed by the DSP blocks (in watts). This value is automatically calculated.
Thermal Power (W)–Total	This shows the estimated power (in watts), based on your inputs. It is the total power consumed by the DSP blocks and is equal to the routing power and block power. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the DSP block configurations of the supported device families, refer to the "DSP Blocks", "Variable Precision DSP Blocks", or "Embedded Multipliers" chapter of the respective device handbook.

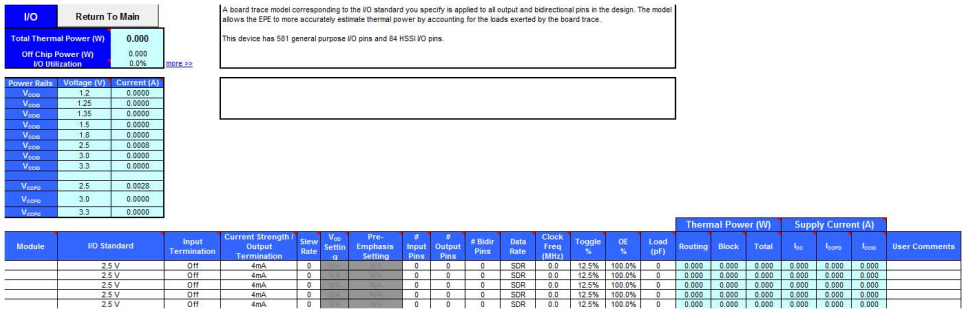
3.5 I/O Worksheet

Each row in the I/O section represents a design module where the I/O pins have the same I/O standard, input termination, current strength or output termination, data rate, clock frequency, output enable static probability, and capacitive load. Enter the following parameters for each design module:

- I/O standard
- Input termination
- Current strength/Output termination
- Slew rate
- Differential output voltage (V_{OD}) setting
- Pre-emphasis setting
- Number of input, output, and bidirectional pins
- I/O data rate
- Clock frequency (f_{MAX}) (in MHz)
- Average pin toggle percentage
- Output enable static probability
- Capacitance of the load

For the EPE spreadsheet version 11.0 onwards, Off Chip Power (W) information is added into the I/O worksheet.

Figure 17. I/O Worksheet of the PowerPlay EPE Spreadsheet



When using the PowerPlay EPE spreadsheet, it is assumed you are using external termination resistors when you design with I/O standards that recommend termination resistors (SSTL and high-speed transceiver logic [HSTL]). If your design does not use external termination resistors, choose the LVTTL/LVCMOS I/O standard with the same VCCIO and similar current strength as the terminated I/O standard. For example, if you are using the SSTL-2 Class II I/O standard with a 16 mA current strength, you must select **2.5 V** as the I/O standard and **16 mA** as the current strength in the PowerPlay EPE spreadsheet.

To use on-chip termination (OCT), select the **Current Strength/Output** option in the EPE spreadsheet.

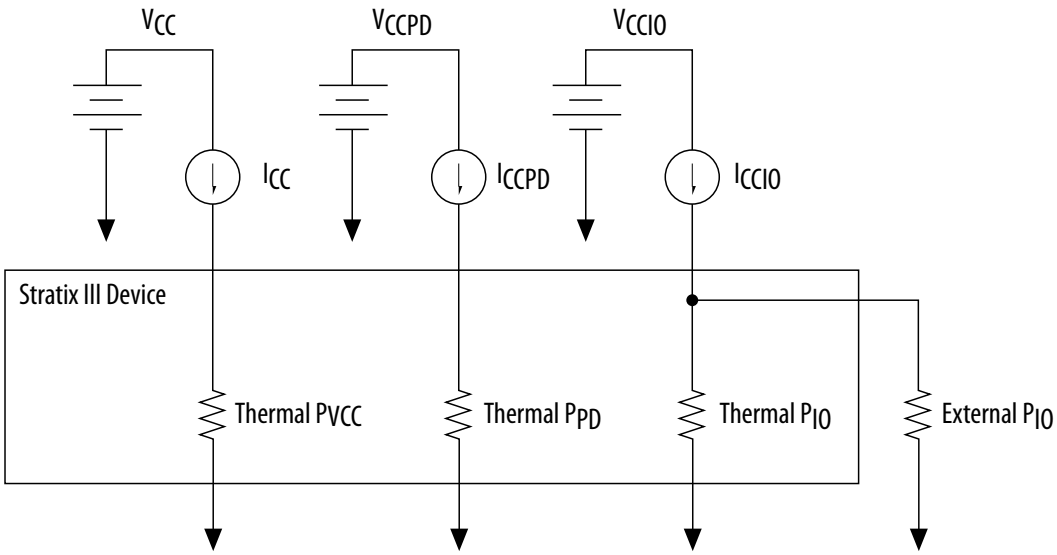
The power reported for the I/O signals includes thermal and external I/O power. The total thermal power is the sum of the thermal power consumed by the device from each power rail, as shown in the following equation.

Figure 18. Total Thermal Power

$$\text{thermal power} = \text{thermal } P_{VCC} + \text{thermal } P_{PD} + \text{thermal } P_{IO}$$

The following figure shows the I/O power consumption. The I_{CCIO} power rail includes both the thermal P_{IO} and the external P_{IO}.

Figure 19. I/O Power Representation



The VREF pins consume minimal current (typically less than 10 µA) and is negligible when compared with the current consumed by the general purpose I/O (GPIO) pins; therefore, the PowerPlay EPE spreadsheet does not include the current for VREF pins in the calculations.

Table 10. I/O Power Rail Information

Column Heading	Description
Power Rails	Power supply rails for the I/O pins.
Voltage (V)	The voltage applied to the specified power rail in Volts (V).
Current (A)	The current drawn from the specified power rail in Amps (A).

Table 11. I/O Worksheet Information

Column Heading	Description
Module	Specify a name for the module in this column. This is an optional value.
I/O Standard	Select the I/O standard used for the input, output, or bidirectional pins in this module from the drop-down list. The calculated I/O power varies based on the I/O standard. For I/O standards that recommend termination (SSTL and HSTL), the PowerPlay EPE spreadsheet assumes you are using external termination resistors. If you are not using external termination resistors, choose the LVTTL/LVCMOS I/O standard with the same voltage and current strength as the terminated I/O standard. To view all the I/O standards in the drop-down list, use the scroll bar.
Input Termination	Select the input termination (on-chip parallel termination [R_T OCT] or on-chip differential termination [R_D OCT]) setting implemented for the input and bidirectional pins in this module.
Current Strength/ Output Termination	Select the current strength or output termination (on-chip serial termination [R_S OCT]) implemented for the output and bidirectional pins in this module. Current strength and output termination are mutually exclusive.

continued...

Column Heading	Description
Slew Rate	Select the slew rate setting for the output and bidirectional pins in this module. Using a lower slew rate setting helps to reduce switching noise but may increase delay.
V_{OD} Setting	Select the V_{OD} for the output and bidirectional pins in this module. If you use a lower voltage, it helps to reduce static power.
Pre-Emphasis Setting	Select the pre-emphasis setting for output and bidirectional pins in this module. Disable the pre-emphasis will reduce dynamic power.
#Input Pins	Enter the number of input pins used in this module. Consider a differential pin pair as one pin.
#Output Pins	Enter the number of output pins used in this module. Consider a differential pin pair as one pin.
#Bidir Pins	Enter the number of bidirectional pins used in this module. When you enable the output enable signal, the I/O pin is treated as an output. When you disable the output enable signal, the I/O pin is treated as an input. An I/O configured as bidirectional but used only as an output consumes more power than an I/O configured as output-only, due to the toggling of the input buffer every time the output buffer toggles (they share a common pin).
Data Rate	Select either **SDR** or **DDR** as the I/O data rate. This indicates whether the I/O value is updated once (single data rate [SDR]) or twice (double data rate [DDR]) in a clock cycle. If the data rate of the pin is DDR, it is possible to set the data rate to SDR and double the toggle percentage. The Quartus II software uses this method to output information.
Clock Freq (MHz)	Enter the clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family. 100 MHz with a 12.5% toggle means that each I/O pin toggles 12.5 million times per second (100 × 12.5%).
Toggle %	Enter the average percentage of input, output, and bidirectional pins toggling on each clock cycle. For input pins used as clocks, the toggle percentage ranges from **0** to **200%** because clocks toggle at twice the frequency. If the pins use DDR circuitry, you can set the data rate to SDR and double the toggle percentage. The Quartus II software uses this method to output information. Typically, the toggle percentage is 12.5%. To be more conservative, you can use a higher toggle percentage.
OE %	Enter the average percentage of time that the: • Output I/O pins are enabled. • Bidirectional I/O pins are outputs and enabled. During the remaining time the: • Output I/O pins are tristated. • Bidirectional I/O pins are inputs. The value you enter must be a percentage between **0** and **100%**.
Load (pF)	Enter the pin loading external to the chip (in pF). This only applies to outputs and bidirectional pins. Pin and package capacitance is already included in the I/O model. Therefore, only include the off-chip capacitance in the Load parameter.
Thermal Power (W)–Routing	This shows the power dissipation due to estimated routing (in watts). Routing power depends on placement-and-routing information, which is a function of design complexity. The values shown represent the routing power based on experimentation of more than 100 designs. For detailed analysis based on your design's routing, use the Quartus II PowerPlay Power Analyzer. This value is automatically calculated.

continued...

Column Heading	Description
Thermal Power (W)–Block	This shows the power dissipation due to internal and load toggling of the I/O (in watts). For accurate analysis based on your design's exact I/O configuration, use the Quartus II PowerPlay Power Analyzer. This value is automatically calculated.
Thermal Power (W)–Total	This shows the total power dissipation (in watts). The total power dissipation is the sum of the routing and block power. This value is automatically calculated.
Supply Current (A)–I_{CC}	This shows the current drawn from the V_{CC} power rail and powers the internal digital circuitry. This value is automatically calculated.
Supply Current (A)–I_{CCPD}	This shows the current drawn from the V_{CCPD} power rail and powers the pre-drive circuitry. This value is automatically calculated.
Supply Current (A)–I_{CCIO}	This shows the current drawn from the V_{CCIO} power rail. Some of this current may be drawn into off-chip termination resistors. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the I/O standard termination scheme of the supported device families, refer to the "I/O Features" chapter of the respective device handbook.

3.6 PLL Worksheet

Intel FPGA devices feature PLLs for general use. Each row in the PLL worksheet of the PowerPlay EPE spreadsheet represents one or more PLLs in the device. Enter the maximum output frequency and the VCO frequency for each PLL. You must also specify whether each PLL is an LVDS, fractional, left/right, or top/bottom PLL.

When a PLL drives source synchronous SERDES hardware, it is referred to as an LVDS PLL. If you are using dedicated transmitters or receivers and are using an LVDS PLL to implement serialization or deserialization, specify an LVDS PLL and enter the power information in the PLL worksheet. LVDS PLLs drive LVDS clock trees and dynamic phase alignment (DPA) buses at the voltage-controlled oscillator (VCO) frequency. If an LVDS PLL drives the LVDS hardware only, enter the appropriate VCO frequency and specify an output frequency of **0 MHz**. If the LVDS PLL also drives a clock to a pin or to the core, specify that clock frequency as the output frequency.

Figure 20. PLL Worksheet of the PowerPlay EPE Spreadsheet

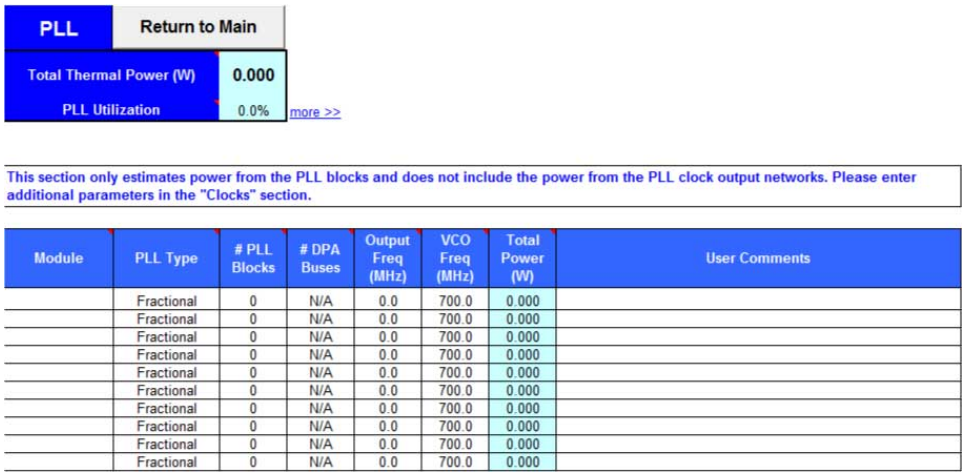


Table 12. PLL Worksheet Information

Column Heading	Description
Module	Specify a name for the PLL in this column. This is an optional value.
PLL Type	Select whether the PLL is a **Fractional**, **Left/Right**, **Top/Bottom**, or an **LVDS** PLL. This option is not applicable for all device families.
# PLL Blocks	Enter the number of PLL blocks with the same specific output frequency and VCO frequency combination.
# DPA Buses	Enter the number of DPA buses in use. DPA is only available for LVDS PLLs. This option is not applicable for all device families.
Output Freq (MHz)	Enter the maximum output frequency of the PLL (in MHz). The maximum output frequency is reported in the Output Frequency column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resource Section**. Select **PLL Usage** and click **Output Frequency**.
VCO Freq (MHz)	Enter the internal VCO operating frequency for this module. The LVDS PLL drives the LVDS clock tree and DPA bus at this frequency. This frequency includes the VCO post scale counter.
Total Power (W)	Shows the estimated combined power for V_{CCA} and V_{CCD} (in watts), based on the maximum output frequency and the VCO frequency you entered. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the PLLs of the supported device families, refer to the "Clock Networks and PLLs" chapter of the respective device handbook.

3.7 Clock Worksheet

Intel FPGA devices support global, regional, or periphery clock networks. The PowerPlay EPE spreadsheet does not distinguish between global or regional clocks because the difference in power is not significant.

Each row in the Clock worksheet of the PowerPlay EPE spreadsheet represents a clock network or a separate clock domain. Enter the following parameters for each design module:

- Clock frequency (in MHz)
- Total fanout for each clock network used
- Global clock enable percentage
- Local clock enable percentage

Figure 21. Clock Worksheet of the PowerPlay EPE Spreadsheet

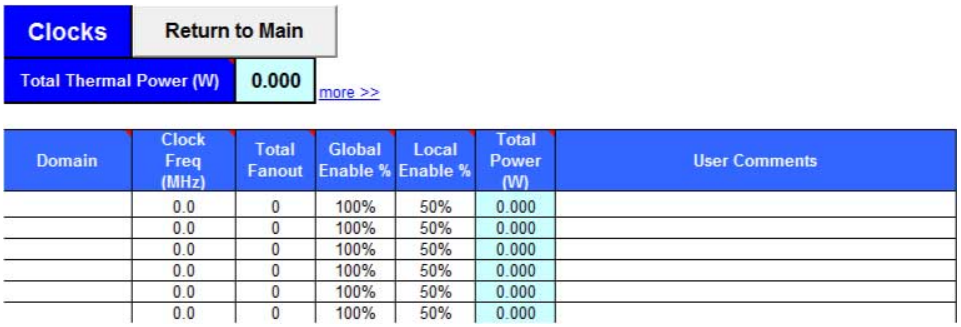


Table 13. Clock Worksheet Information

Column Heading	Description
Domain	Specify a name for the clock network in this column. This is an optional value.
Clock Freq (MHz)	Enter the frequency of the clock domain. This value is limited by the maximum frequency specification for the device family.
Total Fanout	Enter the total number of flipflops and RAM, DSP, and I/O blocks fed by this clock. The number of resources driven by every global clock and regional clock signal is reported in the Fan-out column of the Quartus II Compilation Report. In the **Compilation Report**, select **Fitter** and click **Resources Section**. Select **Global and Other Fast Signals** and click **Fan-out**.
Global Enable %	Enter the average percentage of time that the entire clock tree is enabled. Each global clock buffer has an enable signal that you can use to dynamically shut down the entire clock tree.
Local Enable %	Enter the average percentage of time that clock enable is high for destination flipflops. Local clock enables for flipflops in ALMs are promoted to LAB-wide signals. When a given flipflop is disabled, the LAB-wide is clock disabled, cutting clock power and the power for down-stream logic. This worksheet models only the impact on clock tree power.
Total Power (W)	This is the total power dissipation due to clock distribution (in watts). This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the clock networks of the supported device families, refer to the "Clock Networks and PLLs" chapter of the respective device handbook.

3.8 HSDI Worksheet

The supported device families feature dedicated circuitry that interface with high-speed differential I/O standards. These are dedicated transmitters and receivers that contain SERDES blocks, respectively. The HSDI worksheet of the PowerPlay EPE spreadsheet is divided into receiver and transmitter sections.

The power calculated in the HSDI worksheet of the PowerPlay EPE spreadsheet only applies to the transmitter serializer block or the receiver deserializer block. The transmitter and receiver are implemented using the ALTLVDS megafunction. The I/O buffer power is calculated in the I/O worksheet and the PLL power is calculated in the PLL worksheet.

Each row in the HSDI worksheet of the PowerPlay EPE spreadsheet represents a separate receiver or transmitter domain. Specify the following parameters for transmitter and receiver domains:

- Data rate (in Mbps)
- Number of channels
- Serialization factor in the transmitter domain
- Deserialization factor in the receiver domain
- Toggle percentage

The receiver power is the same whether or not you use the DPA circuitry.

Figure 22. HSDI Worksheet of the PowerPlay EPE Spreadsheet

HSDI | Return to Main

Total Thermal Power (W)	0.000
Tx Channel Utilization	0.0%
Rx Channel Utilization	0.0%

more >>

This section only estimates power within the SERDES blocks and does not include the I/O power nor PLL power. Please enter the appropriate parameters in the "IO" section for I/O power, and "PLL" section for PLL power.

Tx Module	Data Rate (Mbps)	# of Channels	Serialization Factor	Toggle %	Total Power (W)	User Comments
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	

Rx Module	Data Rate (Mbps)	# of Channels	Deserialization Factor	Toggle %	Total Power (W)	User Comments
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	
	0	0	7	50.0%	0.000	

Table 14. HSDI Worksheet Information

Column Heading	Description
TX/RX Module	Specify a name for the module in this column. This is an optional value.
Data Rate (Mbps)	Enter the maximum data rate in Mbps of the receiver or transmitter module.
# of Channels	Enter the number of receiver and transmitter channels running at the above data rate. This number must be an integer value from **0** to **156**.
Serialization Factor/ Deserialization Factor	Enter the number of parallel data bits for each serial data bit. This number must be an integer value from **1** to **10**.
Toggle %	Enter the average percentage of toggling on each clock cycle. The toggle percentage ranges from **0** to **100%**. The default toggle percentage is **50%**.
Total Power	This shows the estimated power (in watts) based on the data rate and number of channels you entered. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the high-speed differential I/O standards of the supported device families, refer to the "High-Speed Differential I/O Interfaces" chapter of the respective device handbook.

3.9 XCVR Worksheet

The supported device families feature dedicated embedded circuitry transceiver channels. This section is only applicable for designs targeting the supported device families.

The power calculated in this section applies to the transceiver blocks, including the channels used and all circuitry used in the clock control unit (CCU). The I/O buffer power and PLL power for the transceivers are included in this section. Transmitters and receivers assume 100 Ω termination.

Each row in the XCVR worksheet represents a separate transceiver domain. Enter the following parameters for each transceiver domain:

- Number of channels
- Protocol used
- Selected V_{CCA} and V_{CCH_GXB} voltage (for Arria V GZ, Stratix IV GX, and Stratix V only)
- Selected V_{CCL_GXB}, V_{CCR}, and V_{CCT} voltage
- Transceiver block operation mode
- Data rate (in Mbps)
- V_{OD} setting (in mV)
- PLL sharing
- PLL type
- Pre-emphasis setting
- Adaptive dispersion control engine (ADCE) setting

- Decision feedback equalization (DFE) setting (for Arria V GZ and Stratix V only)
- Equalizer stages (for Arria V GZ and Stratix V only)
- Width of the parallel data bus
- For certain modes, you must specify if you use the byte serializer, rate match FIFO setting, and 8B/10B encoder features.

Figure 23. XCVR Worksheet of the PowerPlay EPE Spreadsheet

XCVR, PCS, HIP	Return to Main
XCVR Thermal Power (W)	0.000
PCS and HIP Thermal Power (W)	0.000
Average XCVR Power per Used Channel (W/Channel)	0.000
XCVR Channel Utilization	0.0%

Each entry in the XCVR page represents a unique transceiver domain with a number of transceiver channels.
Power of transceiver I/O pins and CMU PLLs is included in this estimate - do not add extra entries to the I/O or PLL pages for transceiver hardware.
However, for TX or Duplex channels using fPLL as Transmit PLL, enter 0 for PLL Sharing, and add appropriate number of PLLs in the PLL worksheet.

XCVR Power Rails	Voltage (V)	Current (A)
V_{CCA}	2.5	0.000
V_{CCA}	3.0	0.000
V_{CCA}	3.3	N/A
V_{CCH_GXB}	1.4	N/A
V_{CCH_GXB}	1.5	0.000
V_{CCR}	0.85	0.000
V_{CCR}	0.9	0.000
V_{CCR}	1.0	0.000
V_{CCR}	1.05	0.000
V_{CCR}	1.1	N/A
V_{CCR}	1.2	N/A
V_{CCT}	0.85	0.000
V_{CCT}	0.9	0.000
V_{CCT}	1.0	0.000
V_{CCT}	1.05	0.000
V_{CCT}	1.1	N/A
V_{CCT}	1.2	N/A
V_{CCA_GTB}	3	N/A
V_{CCH_GTB}	1.5	N/A
V_{CCL_GTB}	1.05	N/A
V_{CCR_GTB}	1.05	N/A
V_{CCT_GTB}	1.05	N/A

XCVR Page Mode	Detailed

Module	# of Channels	Protocol	V_{CCA} Voltage	V_{CCH_GXB} Voltage	V_{CCL_GXB}, V_{CCR}, and V_{CCT} Voltage	Operation Mode	Data Rate (Mbps)	V_{OD} Setting	PLL Sharing	PLL Type
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	800	1	CMU
	0	Basic	2.5	1.5	0.85	Receiver and Transmitter	4250	180	1	CMU

Pre-Emphasis Setting														
Pre-Tap	First Post-Tap	Second Post-Tap	ADCE	DFE	Equalizer Stages	Parallel Data Width	Byte Serializer Used	Rate Match FIFO Used	8B10B Encoder Used	Channel Power (W)	CCU Power (W)	XCVR Power (W)	PCS and HIP Power (W)	User Comments
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	
0	0	0	Off	Off	Bypass Stages 234	32	Yes	Yes	Yes	0.000	0.000	0.000	0.000	

Table 15. XCVR Worksheet Information

Column Heading	Description
Module	Specify a name for the module in this column. This is an optional value.
# of Channels	Enter the number of channels used in this transceiver domain. These channels are grouped together in one transceiver block or two adjacent transceiver blocks and clocked by one or more common PLLs. The number of channels allowed in each domain depends on the selected protocol.
Protocol	Enter the communication protocol or standard these transceivers implement. Choose from the drop-down list. For custom protocols not listed in the drop-down list, choose **Basic** or **Basic (PMA Direct)** protocol and adjust other settings appropriately.
V_{CCA} Voltage	Enter the voltage of the V_{CCA} power rail used by the transceiver block. This option is available for Arria V GZ, Stratix IV GX, and Stratix V devices only.
V_{CCH_GXB} Voltage	Enter the voltage of the V_{CCH_GXB} power rail used by the transceiver block. This option is available for Arria V GZ, Stratix IV GX, and Stratix V devices only.
V_{CCL_GXB}, V_{CCR}, and V_{CCT} Voltage	Select the voltage for the V_{CCL_GXB}, V_{CCR}, and V_{CCT} power rails.
Operation Mode	Enter the operation mode implemented by the transceiver block. Options include: • **Receiver and Transmitter** • **Receiver only** • **Transmitter only**
Data Rate (Mbps)	Enter the transceiver data rate (in Mbps).
V_{OD} Setting	Enter the V_{OD} setting (mV) of the gigabit transceiver block (GXB) transmitter channel PMA. It is assumed that the transmitter uses a termination resistance of 100 Ω .
PLL Sharing	Specify the number of transmitter PLLs that are shared by the transceiver channels on the same row. This value is ignored for Receiver-only channels. For device families that support using fPLLs as transmitter PLLs such as channels on a given row use only fPLLs as transmitter PLLs, enter 0 for PLL sharing and add appropriate number of fPLLs in the PLL worksheet.
PLL Type	Select **ATX** or **CMU** for device families that support multiple transmitter PLL types. If the channel uses fPLL as transmitter PLL, enter 0 for PLL sharing and add appropriate number of PLLs in the PLL worksheet.
Pre-Emphasis Setting–Pre-Tap	Enter the pre-emphasis pre-tap setting used by the transmitter. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
Pre-Emphasis Setting–First Post-Tap	Enter the pre-emphasis first post-tap setting used by the transmitter. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.

continued...

Column Heading	Description
Pre-Emphasis Setting–Second Post-Tap	Enter the pre-emphasis second post-tap setting used by the transmitter. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
ADCE	Enter whether the ADCE is turned **On** or **Off**. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
DFE	Specify DFE mode as **Manual** or **Triggered Adaption** when DFE is used. The DFE is turned **Off** by default. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
Equalizer stages	Select **All stages Enabled** or **Bypass Stages 234**. Bypass equalizer stages 2, 3, and 4 reduce power consumption of the transceiver channels.
Parallel Data Width	Enter the width of the parallel data bus going into each GXB transmitter channel PCS and coming out of each GXB receiver channel PCS. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
Byte Serializer Used	Enter whether or not the byte SERDES is used. If the byte serializer is used, the transceiver is in double-width mode. If it is not used, the transceiver is in single-width mode. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
Rate Match FIFO Used	Enter whether or not the rate matching FIFO is used. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
8B10B Encoder Used	Enter whether or not 8B/10B encoder/decoder is used. To enter this parameter, set the **XCVR Page Mode** section to **Detailed**.
Channel Power (W)	This shows the total power of the GXB transmitter channel PMA and GXB receiver channel PMA blocks for all channels (in watts). This value is automatically calculated.
CCU Power (W)	This shows the total power of the GXB PLLs and control circuitry for all channels (in watts). This value is automatically calculated.
XCVR Power (W)	This shows the sum of the channel power and CCU power (in watts). This value is automatically calculated.
PCS/HIP Power (W)	This shows the total power of the GXB transmitter channel PCS, GXB receiver channel PCS, and PCIe hard IP blocks for all channels (in watts). This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

Values of some settings in the XCVR worksheet are restricted for one of the following reasons:

- The setting value is restricted due to the selections made for other settings.
- Changing the setting would not have a significant impact on power, given the selected values of other settings.

For more information about the transceiver architecture of the supported device families, refer to the "Transceiver Architecture" chapter in the respective device handbook.

3.10 HMC Worksheet

The EPE spreadsheet version 11.1 introduces the HMC worksheet. Each row in the HMC worksheet represents a single instance of the HMC interface. Enter the information for HMC instances in different rows, even if some of the HMC instances have the same configuration. Specify the following information for each HMC instance:

- Clock frequency (in MHz)
- DRAM interface width
- Number of command port
- Fabric interface width

The HMC worksheet is only applicable to Arria V and Cyclone V device families with HMC controllers.

Figure 24. HMC Worksheet of the PowerPlay EPE Spreadsheet

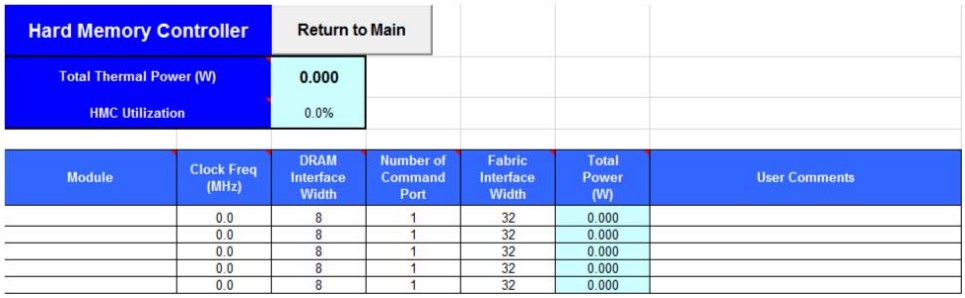


Table 16. HMC Worksheet Information

Column Heading	Description
Module	Specify a name for the HMC module in this column. This is an optional value.
Clock Freq (MHz)	Enter the clock frequency (in MHz). This value is limited by the maximum frequency specification for the device family.
DRAM Interface Width	Enter the memory interface width used in this module. The memory interface width is the number of DQ pins of the memory device.
Number of Command Port	Enter the number of fabric interface command ports used in this module. The fabric interface command port is configured to accept both read and write commands, write only, or read only.
Fabric Interface Width	Enter the number of fabric interface data ports used in this module. The fabric interface width is the number of data ports that transfer data signals from the FPGA fabric to the HMC and vice versa.
Total Power (W)	Total power dissipation due to HMC distribution (in watts). This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

For more information about the HMCs of the supported device families, refer to the "External Memory Interfaces" chapter of the respective device handbook.

3.11 IP Worksheet

The IP worksheet is an IP design entry feature that automatically fills in resource usage of commonly used IP designs , automatically allocates appropriate resources for the selected IP and calculates power consumption.

The IP worksheet is not available for MAX 10 devices.

Each row in the IP worksheet represents a separate IP domain. For the EPE spreadsheet version 11.0 and later, supported IPs are external memory interfaces (EMIs), including DDR2 and DDR3, QDR II, and RLDRAM II in different configurations (for example, x9, x18, x36, and x72).

Enter the following parameters for each IP domain:

- Type of IP
- Data width in bits
- Clock frequency (in MHz)
- Enable percentage
- Total power in watts

Figure 25. IP Worksheet of the PowerPlay EPE Spreadsheet

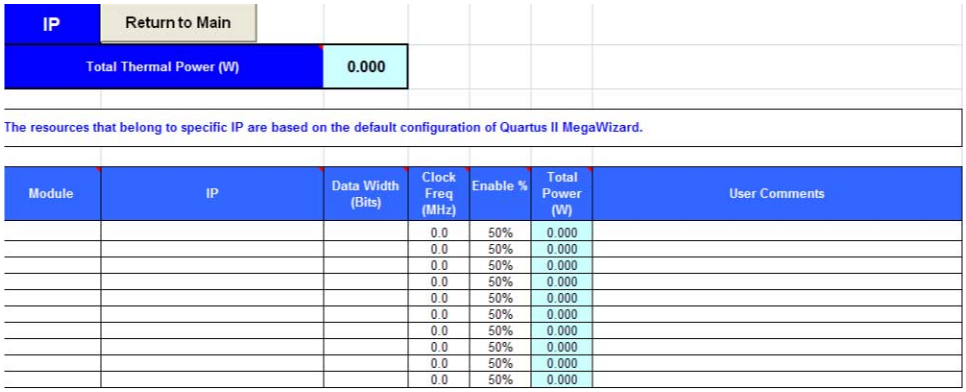


Table 17. IP Worksheet Information

Column Heading	Description
Module	Specify a name for the module in this column. This is an optional value.
IP	Select a supported IP type for a specific device family. Each device family has different supported IPs.
Data Width (Bits)	The interface data width of the specific IP (in bits).
Clock Freq (MHz)	This shows the clock frequency based on the IP type selected. This value is automatically selected.
Enable %	Enter the percentage of enable for the selected IP. The range allowed is from 0% (off) to 100% (fully enabled).
Total Power (W)	Total power consumed by the selected IP. This value is automatically calculated.
User Comments	Enter any comments. This is an optional entry.

Related Links

Intel FPGA External Memory Interface Solutions Center

3.12 HPS Worksheet

The HPS worksheet is only applicable to Arria V and Cyclone V device families with HPS. The HPS static power will be turned on once the SoC device is selected.

Figure 26. HPS Worksheet of the PowerPlay EPE Spreadsheet

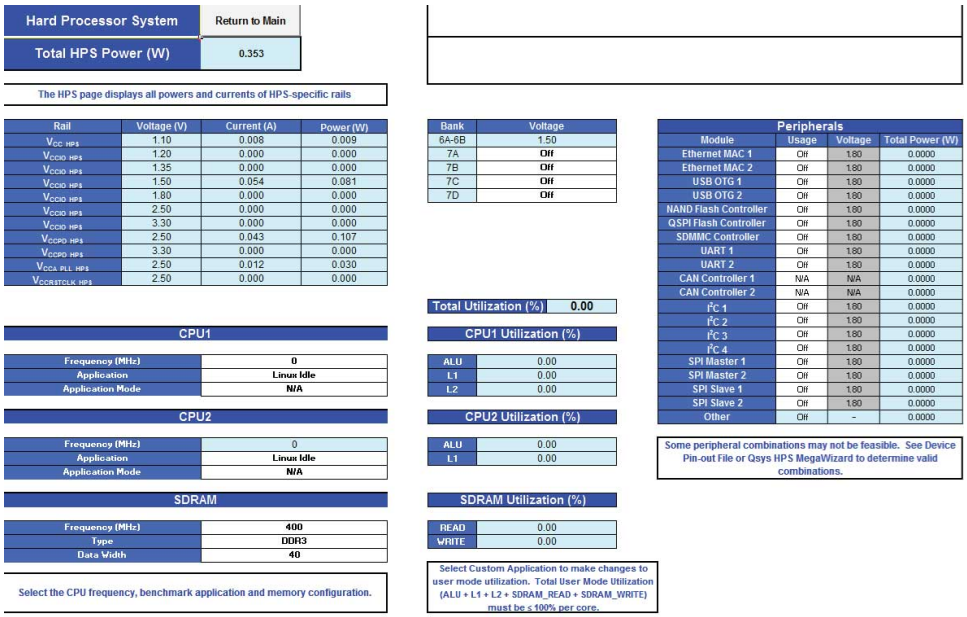


Table 18. HPS Worksheet Information

Module	Parameters	Description
CPU1/2	Frequency	Enter the operating frequency of the CPU.
	Application	Select the available benchmark application. To make changes to user mode utilization, select custom application. Total User mode utilization (ALU +L1 + L2 +SDRAM_READ +SDRAM_WRITE) must be < 100% per core.
	Application Mode	Select the available application mode. This setting is only applicable to some applications.
SDRAM	Frequency	Enter the operating frequency of the selected DDR protocol used.
	Type	Select the DDR protocol used.
	Data Width	Select the width of the data lines (in bits).
Peripherals	Usage	Select **On** for module in use. Turn on the appropriate voltage for one of the I/O banks before selecting the module.
	Voltage	Select the voltage used for this module.

3.13 Report Worksheet

The Report worksheet shows all the information and power estimation results from the PowerPlay EPE spreadsheet. You can find the power supply recommendations in the Power Supply Current (A) section, which describes all the power supply requirements for the device that your design uses in the Min Current Requirement (A) and the User Mode Current Requirement (A) columns.

The Min Current Requirement (A) column is not available for MAX 10 devices.

3.13.1 Static Power and Dynamic Current per Voltage Rail

The Report worksheet shows all the information and power estimation results from the PowerPlay EPE spreadsheet. You can find the power supply recommendations in the Power Supply Current (A) section, which describes all the power supply requirements for the device that your design uses in the Min Current Requirement (A) and the User Mode Current Requirement (A) columns.

Figure 27. Separate Static and Dynamic Current in Power Supply Current Section

Power Supply Current (A)	Min Current Requirement (A)	User Mode Current Requirement (A)			Power Regulator Settings
		Static Current (A)	Dynamic Current (A)	Total Current (A)	Regulator Group
I_{CC} (1.10V)	1.719	0.387	1.331	1.719	1
I_{CCA_PLL} (2.50V)	0.047	0.011	0.036	0.047	2
I_{CCD_PLL} (N/A)	N/A	N/A	N/A	N/A	
I_{CCBAT}	9.000E-06	9.000E-06	0.000E+00	9.000E-06	2
I_{CCIO}	0.494	0.408	0.086	0.494	
I_{CCIO} (1.2V)	N/A	0.000	0.024	0.024	2
I_{CCIO} (1.25V)	N/A	0.000	0.000	0.000	
I_{CCIO} (1.35V)	N/A	0.000	0.000	0.000	

3.13.2 Power Up Current

In some device families, the power up current can be larger than the dynamic current required in the I/O worksheet. For example, in Stratix III and Stratix IV devices, the I_{CCPD} value on the I/O worksheet is different than the Minimum current requirement for I_{CCPD} in Report worksheet.

Intel provides the minimum current required for the V_{CCPD} power rail for each voltage supply used, but is not dependent on how many banks use that voltage supply.

To estimate the power up current, use the Report worksheet and compare the minimum current requirement with user mode current requirement.

3.13.3 Power Breakout for Multiple Voltage Supplies

For V_{CCIO} and V_{CCPD}, the minimum current requirement reported for I_{CCIO} and I_{CCPD} respectively has the same value for each voltage rail used in your design.

These values are based on all I/O pins in the device being powered by the same voltage rail, thus the minimum current requirement is repeated for each unique voltage rail used by V_{CCIO} and V_{CCPD}.

To better estimate the minimum current requirements for I_{CCIO} and I_{CCPD} based on your device and design usage, you can use the following equations:

- [(Number of I/O pins powered by V_{CCIO} voltage) / (number of total I/O pins in the device)] × (Minimum supply current) × (1.10)
- [(Number of I/O pins powered by V_{CCPD} voltage) / (number of total I/O pins in the device)] × (Minimum supply current) × (1.10)

Repeat the formula for each V_{CCIO} voltage and V_{CCPD} voltage used in your design. The number of I/O pins powered by V_{CCIO} and V_{CCPD} voltage represents the count of both used and unused I/O pins in I/O banks powered by a particular voltage. The minimum supply current is the value provided in the power estimation tools for I_{CCIO} and I_{CCPD}.

The 1.10 scaling factor is provided as additional guardband and must be included for your power estimation.

3.13.4 Power Regulator Settings

Regulator groups consist of rails that can be combined and supplied by a single regulator. A manual entry here can move a rail from one group to another or create a new group. This may be necessary to correct grouping errors that may occur.

Related Links

Power Tree Design on page 15

3.14 Enpirion Worksheet

Enpirion power devices are available to satisfy the power requirements for the power rails on Intel FPGA devices. Power devices are selected based on load current, input and output voltages, and power-delivery configuration.

Each row in the Regulator Selection table represents the power solution for a single power group. The power groups are created by combining rails that can be allowably supplied from the same source. Enpirion device selection is enabled when the Main worksheet for the Maximum Power Characteristics and the Regulator Group section of the Report worksheet are set up correctly with no grouping errors.

In the following figure, a 12-V off-line regulator supplies input power for Groups 1 and 5. The 3-V regulator supplying Group 5 also acts as an intermediate bus supplying input power for Groups 2, 3, and 4.

Figure 28. Enpirion Worksheet of the PowerPlay EPE Spreadsheet

Regulator Selection

Group	Regulator Input Voltage (V)	Regulator Current Draw (A)	Voltage (V)	Load Current (A)	Load Current Margin	Parent Group	Regulator Type	POK	Suggested Enpirion Part	Pin Compatible Parts	Note
1	12.00	0.978	0.90	11.082	30.00%	0	Switcher	No	EN23F0QI		Derating might be required based on system thermal characteristics. Review the Data sheet for more details.
2	3.00	1.167	2.50	1.190	30.00%	5	Switcher	No	EN6337QI	EN6347QI	
3	3.00	0.784	1.00	1.998	30.00%	5	Switcher	No	EN6337QI	EN6347QI	
4	3.00	0.987	1.50	1.678	30.00%	5	Switcher	No	EN5329QI	EN5319QI EN5339QI	
5	12.00	0.928	3.00	3.157	30.00%	0	Switcher	No	EN2342QI	EN2362QI	
6	N/A	N/A	N/A	N/A	30.00%	0	Switcher	No	N/A	N/A	N/A
7	N/A	N/A	N/A	N/A	30.00%	0	Switcher	No	N/A	N/A	N/A
8	N/A	N/A	N/A	N/A	30.00%	0	Switcher	No	N/A	N/A	N/A

Table 19. Enpirion Worksheet Information

Column Heading	Description
Group	Compatible rails are combined in order to minimize the number of regulators required. For additional information, refer to the Report worksheet. See also Grouping Errors on the Main worksheet.
Regulator Input Voltage (V)	Enter the input voltage here. The output voltage will be derived from this voltage. This field is filled automatically when non-zero Parent Group is specified.

continued...

Column Heading	Description
Load Current Margin	Margin can be added to account for component variability. It is recommended to retain the default 30% to assure the thermal capability of the solution over the full range of device variation and operating conditions. However, in certain cases when characteristics and conditions are fully defined, reducing the margin may lead to a more cost-effective solution. Exercise caution when changing these values.
Parent Group	If one of the group voltages is to be used as an intermediate bus voltage, enter the group number here.
Regulator Type	In some cases, a linear regulator (LDO) may be a good choice to supply one of the group voltages. The efficiency of an LDO is the ratio of output voltage to input voltage. In the figure, Group 2 can be efficiently supplied by an LDO. If desired, select **Linear** in the row for Group 2.
POK	Select **Yes** to select a regulator with a Power OK (**POK**) output to assist with sequencing.
Suggested Enpirion Part	Suggested Enpirion part is automatically populated with the part number of the device that most closely matches the **Load Current (A)**, **Regulator Type** and **POK** selections. The dropdown can be used to optionally select devices with equivalent or higher current capabilities.
Pin Compatible Parts	Pin compatible parts are devices with equivalent or higher current capabilities that can be placed on the same PCB footprint as the **Suggested Enpirion Part**. Additional components or changes to component values may be required when using a pin compatible part.

Related Links

- Power Tree Design on page 15
- Report Worksheet on page 41

4 Factors Affecting the PowerPlay Early Power Estimator Spreadsheet Accuracy

Many factors can affect the estimated values displayed in the PowerPlay EPE spreadsheet. In particular, the input parameters entered concerning toggle rates, airflow, temperature, and heat sinks must be accurate to ensure that the system is modeled correctly in the PowerPlay EPE spreadsheet.

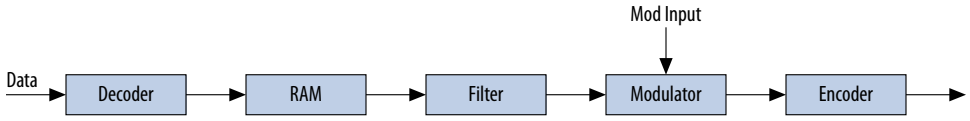
4.1 Toggle Rate

The toggle rates specified in the PowerPlay EPE spreadsheet can have a large impact on the dynamic power consumption displayed. To obtain an accurate estimate, you must input toggle rates that are realistic. Determining realistic toggle rates requires knowing what kind of input the FPGA is receiving and how often it toggles.

To get an accurate estimate if the design is not complete, isolate the separate modules in the design by functionality and estimate the resource usage along with the toggle rates of the resources. The easiest way to accomplish this is to leverage previous designs to estimate the toggle rates for modules with similar functionality.

The input data in the following figure is encoded for data transmission and has a roughly 50% toggle rate.

Figure 29. Decoder and Encoder Block Diagram



In this case, you must estimate the following:

- Data toggle rate
- Mod input toggle rate
- Resource estimate for the Decoder module, RAM, Filter, Modulator, and Encoder
- Toggle rate for the Decoder module, RAM, Filter, Modulator, and Encoder

You can generate these estimates in many ways. If you used similar modules in the past with data inputs of roughly the same toggle rate, you can leverage that information. If MATLAB simulations are available for some blocks, you can obtain the toggle rate information. If the HDL is available for some of the modules, you can simulate them.

If the HDL is complete, the best way to determine toggle rate is to simulate the design. The accuracy of toggle rate estimates depends on the accuracy of the input vectors. Therefore, determining whether or not the simulation coverage is high gives you a good estimate of how accurate the toggle rate information is.

The Quartus II software can determine toggle rates of each resource used in the design if you provide information from simulation tools. Designs can be simulated in many different tools and the information provided to the Quartus II software through a Signal Activity File (`.saf`). The Quartus II PowerPlay Power Analyzer provides the most accurate power estimate. You can import the Comma-separated Value file (`.csv`) from the Quartus II software into the PowerPlay EPE spreadsheet for estimating power after your design is complete.

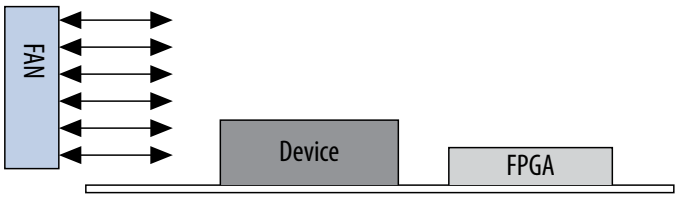
4.2 Airflow

It is often difficult to place the device adjacent to the fan providing the airflow. The path of the airflow might traverse a length on the board before reaching the device, thus diminishing the actual airflow the device receives. The following figure shows a fan that is placed at the end of the board. The airflow at the FPGA is weaker than the airflow at the fan.

Figure 30. Airflow and FPGA Position

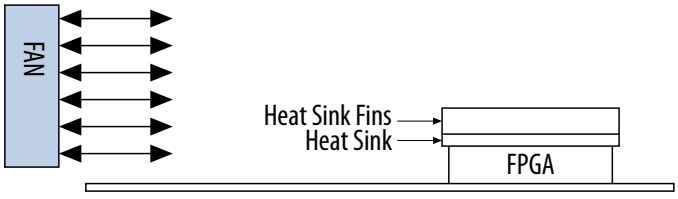
You must also consider blocked airflow. The following figure shows a device blocking the airflow from the FPGA, significantly reducing the airflow seen at the FPGA. The airflow from the fan also has to cool board components and other devices before reaching the FPGA.

Figure 31. Airflow with Component and FPGA Positions



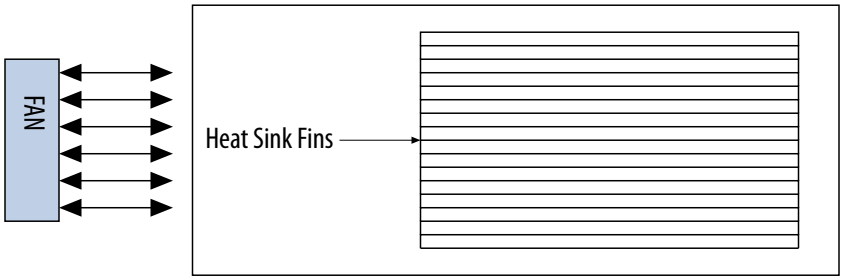
If you are using a custom heat sink, you do not need to enter the airflow directly into the PowerPlay EPE spreadsheet but it is required to enter the θ_{SA} value for the heat sink with the knowledge of what the airflow is at the device. Most heat sinks have fins located above the heat sink to facilitate airflow. The following figure shows the FPGA with a heat sink.

Figure 32. Airflow and Heat Sinks



When placing the heat sink on the FPGA, the direction of the fins must correspond with the direction of the airflow. A top view shows the correct orientation of the fins.

Figure 33. Heat Sink (Top View)



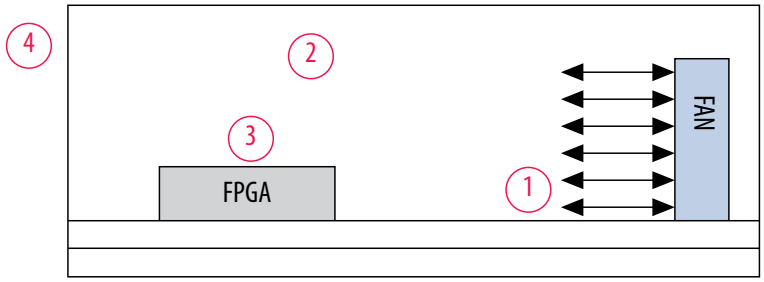
These considerations can influence the airflow at the device. When entering information into the PowerPlay EPE spreadsheet, you have to consider these implications to get an accurate airflow value at the FPGA.

4.3 Temperature

To calculate the thermal information of the device correctly, you are required to enter the ambient air temperature for the device in the PowerPlay EPE spreadsheet. Ambient temperature refers to the temperature of the air around the device. The temperature of the air around the device is usually higher than the ambient temperature outside of the system. To get an accurate representation of ambient temperature for the device, you must measure the temperature as close to the device as possible with a thermocouple device.

Entering the incorrect ambient air temperature can drastically alter the power estimates in the PowerPlay EPE spreadsheet. The following figure shows a simple system with the FPGA housed in a box. In this case, the temperature is very different at each of the numbered locations.

Figure 34. Temperature Variances



For example, location 3 is where the ambient temperature pertaining to the device should be obtained for input into the PowerPlay EPE spreadsheet. Locations 1 and 2 are cooler than location 3 and location 4 is likely close to 25 °C if the ambient temperature outside the box is 25 °C. Temperatures close to devices in a system are often in the neighborhood of 50–60 °C but the values can vary significantly. To obtain accurate power estimates from the PowerPlay EPE spreadsheet, you must get a realistic estimate of the ambient temperature near the FPGA device.

4.4 Heat Sink

The following equations show how to determine power when using a heat sink.

Figure 35. Total Power

$$P = \frac{T_J - T_A}{\theta_{JA}}$$

Figure 36. Junction–to–Ambient Thermal Resistance

$$\theta_{JA\ TOP} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

You can obtain the θ_{JC} value that is specific to the FPGA from the data sheet. The θ_{CS} value refers to the material that binds the heat sink to the FPGA and is approximated to be 0.1 °C/W. You can obtain the θ_{SA} value from the manufacturer of the heat sink. Ensure that you obtain this value for the right conditions for the FPGA which include analyzing the correct heat sink information at the appropriate airflow at the device.

A Additional Information for PowerPlay Early Power Estimator User Guide

A.1 Document Revision History for PowerPlay Early Power Estimator User Guide

Date	Version	Changes
February 2017	2017.02.21	Rebranded as Intel.
January 2015	2015.01.20	Added support for MAX 10 devices.
July 2014	2014.07.25	• Updated changing the macro security level in Microsoft Excel 2010 • Updated "Main Worksheet", "Logic Worksheet", "RAM Worksheet", "I/O Worksheet", "PLL Worksheet", "XCVR Worksheet", "HPS Worksheet", and "Report Worksheet". • Added "Enpirion Worksheet" section.
June 2013	8.0	• Updated "PowerPlay Early Power Estimator Overview". • Added "HPS Worksheet" section. • Updated "Thermal Power", "Power Supply Current", "Logic Worksheet", "XCVR Worksheet", and "IP Worksheet" sections. • Updated Figure 3–1, Figure 3–2, Figure 3–3, Figure 3–9, Figure 3–11, Figure 3–12, Figure 3–13, Figure 3–15, Figure 3–16, and Figure 3–17. • Updated Table 2–1, Table 2–2, Table 3–1, Table 3–2, Table 3–4, Table 3–5, Table 3–6, Table 3–13, Table 3–15, and Table 3–16. • Added Table 3–17. • Removed power savings information in "Logic Worksheet", "RAM Worksheet", "DSP Worksheet", "I/O Worksheet", "PLL Worksheet", "Clock Worksheet", and "HSDI Worksheet". • Removed "Report Power Savings for Each Functional Block" section in the "Report Worksheet".
July 2012	7.1	Updated Table 3–4 and Table 3–5.
June 2012	7.0	• Updated "XCVR Worksheet" section. • Updated Figure 3–1. • Updated Table 3–13.
January 2012	6.0	• Added "HMC Worksheet" section. • Updated "IP Worksheet" section. • Updated Figure 3–1, Figure 3–2, Figure 3–21, and Table 3–2. • Added Cyclone V device. • Added Microsoft Excel 2010 support in "System Requirements" and "Download and Install the PowerPlay Early Power Estimator" sections.
August 2011	5.0	• Updated for the Quartus II software version 11.0 release to include Arria V devices. • Removed PowerPlay EPE spreadsheet version, power model status, and supported feature information to the PowerPlay Early Power Estimators (EPE) and Power Analyzer page of www.altera.com.

continued...

Date	Version	Changes
May 2011	4.0	• Added "PLL Worksheet" section. • Updated "Report Worksheet" section. • Updated Figure 3–1, Figure 3–9, Figure 3–11, Figure 3–12, Figure 3–13, Figure 3–15, Figure 3–16, and Figure 3–18.
December 2010	3.0	• Updated for the Quartus II software version 10.0 release. • Added information about Arria II GZ devices. • Updated Table 1–1, Table 1–2, and Table 1–3.
July 2010	2.0	Updated for the Quartus II software version 10.0 release: • Added Stratix V device. • Added "Report Worksheet". • Updated "System Requirements", "Download and Install the PowerPlay Early Power Estimator", "Entering Information into the PowerPlay Early Power Estimator", and "Estimating Power Consumption" • Combining all the worksheets into "PowerPlay Early Power Estimator Worksheets" chapter. • Updated Table 1–2, Table 1–3, Table 7–2, and Table 11–1. • Updated Figure 3–1. • Minor text edits.
January 2010	1.1	Updated Table 1–2 and Table.
November 2009	1.0	Initial release.