

MATLAB SIMULINK/MODELSIM CO-SIMULATION TUTORIAL

You can find the original MathWorks' tutorial at <http://www.mathworks.se/access/helpdesk/help/toolbox/edalink/ug/bsctzv -63.html>.

The following is a summary of all necessary steps required to run Simulink/Modelsim co-simulation based on the aforementioned MathWorks' tutorial which has been complemented with tips and hints based on my personal experience with Simulink/Model co-simulation feature.

1. Open Simulink by entering "simulink" in the MATLAB shell.
2. In "Simulink Library Browser" go to "EDA simulator Link MQ" (MQ denotes Modelsim co-simulation block). If you do not see the "EDA Simulator Link" tab in "Simulink Library" it either means that this feature has not been installed (if you are using 32-bit version of MATLAB) or you are using 64-bit version of MATLAB in which case you will not be able to use the Simulink/Modelim co-simulation feature as it is only available in 32-bit version.
3. Place "HDL Cosimulation" component(s) in your Simulink project window.
4. In the MATLAB shell type in "vsim('socketsimulink', 4449)". It will open a socket connection on port 4449 (you can change the port number if you wish) between Simulink and Modelsim.
5. In Modelsim create a project which will include all Verilog modules that you will be instantiating in a Simulink project (include also modules' files which are instantiated inside the main Verilog modules that will be run in the Simulink project).
6. Compile all Verilog files and type in in the Modelsim shell "vsimulink work.module_1 work.module_2 ... work.module_x" where:
 - module_1
 - module_2
 - ...
 - module_xdenote the names of Verilog modules which you want to instantiate in the Simulink project.
7. In the Simulink project window double click on the "HDL Cosimulation" block(s) which you created in Step 3. and in "Function Block Parameters HDL Cosimulation" window which will show up go to "Connection" tab and select "Socket" from a drop-down list next to "Connection method" option and click "Apply".

****** Note: You have to do both steps 6 and 7 in order to enable co-simulation feature between Simulink and Modelsim. The order of performing steps 6 and 7 does not matter but you need to complete both step, otherwise you will be***

prompted with various connection errors/warning pop-ups and as a result you will not be able to run a simulation.

8. Double click the "HDL Cosimulation" block(s) to open again the "Function Block Parameters HDL Cosimulation" window and go to 'Ports' tab. You can either enter manually all input and output ports of your Verilog module(s) or you can use a very convenient feature, called "Auto Fill" - a button in the left top corner of "Ports" sub-window. which will bring up all the ports defined in your Verilog module. After you click on "Auto Fill" button in the window that will show up enter the name of the Verilog module and click "OK". It will cause all the ports to appear in "Ports" window.

****** Note: "Auto Fill" only appends the list of ports from the Verilog module (it does not update the list) so if you need to make a change to ports inside your Verilog after you updated the ports' list using "Auto Fill" option or after you entered the ports manually you will have to delete all the ports from the previous usage of "Auto Fill" option (after each change to Verilog file perform actions in Step 6 to render all changes effective).***

9. If your Verilog module has a clock input copy the name of the clock input path from a field under "Full HDL Name" column in "Ports" window and paste it in "Clocks" window which is accessed through a second tab following "Ports" tab. Delete the corresponding clock entry in "Ports" window unless you want to use external (Simulink) signal for a clock in which case ignore Step 9 all together.
10. "Timescales" tab determines the relationship between Simulink and Modelsim simulation time units. Make sure to select the right option for your simulation setup. The time units' relationship will be used as a base reference for interpretation of the value you enter in "Period" ("Clocks" tab) or "Sample Time" ("Ports" tab) fields next to a specific port. For example, if you select that "1 second in Simulink corresponds to 1 second in the HDL simulator" Modelsim will use absolute time values entered in Simulink Ports' "Sample Time"/ "Clocks' "Period" (for clock inputs) . For instance, if you enter 20e-6 in "Period" field in "Clocks" section the period of a clock in Modelsim will be also 20e-6 (20us). However, if you do not want to enter a base time unit in every "Sample Time" / "Period" field, for instance in the previous example "e-6", you can use relative relationship between Modelsim and Simulink time units by selecting "1 second in Simulink corresponds to 1 us in the HDL simulator". By doing that, you only have to enter a number of the based time units in Simulink "Sample Time"/"Period" fields and Modelsim will interpret this value in a given base time unit for you - for example, if you enter 20 in "Period" field in "Period" section Modelsim will produce a clock with 20us period.
11. If you use a fixed-point representation of Verilog module's outputs select either "Signed" or "Unsigned" option under "Data Type" in "Ports" section and then enter the number of fractional bits out of the total number of the port's bits in "Fractional Length" field in "Ports" Section.

12. The last step concerns specification how the input signals from Simulink to "HDL Cosimulation" block(s) will be interpreted. For every Verilog module's input instantiate a "Data Type Conversion" block from Simulink->Commonly Used Blocks library in the Simulink project. Double click on the created "Data Type Conversion" block(s) and click ">>" button to unfold the number representation interpretation options. In "Mode" drop-down list select "Fixed-point" and specify "Signedness", "Word length" and "Fraction length" options. Connect all "Data Type Conversion" block(s) to "HDL Cosimulation" block(s)' inputs.
13. Now you can run a co-simulation between Modelsim and Simulink by pressing "Start Simulation" button in Simulink. You can view Verilog module's signals in the Modelsim waveform viewer by performing the following steps:
 - add a desired Verilog module's signal by clicking on it and selecting "Add to Wave"->"Selected Signals" option
 - reset Modelsim simulation by clicking on "Restart" button next to the simulation time field in Modelsim and run the simulation again by pressing "Start Simulation" button in Simulink.